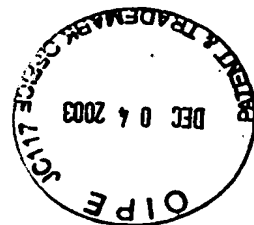


FIG. 1
PRIOR ART



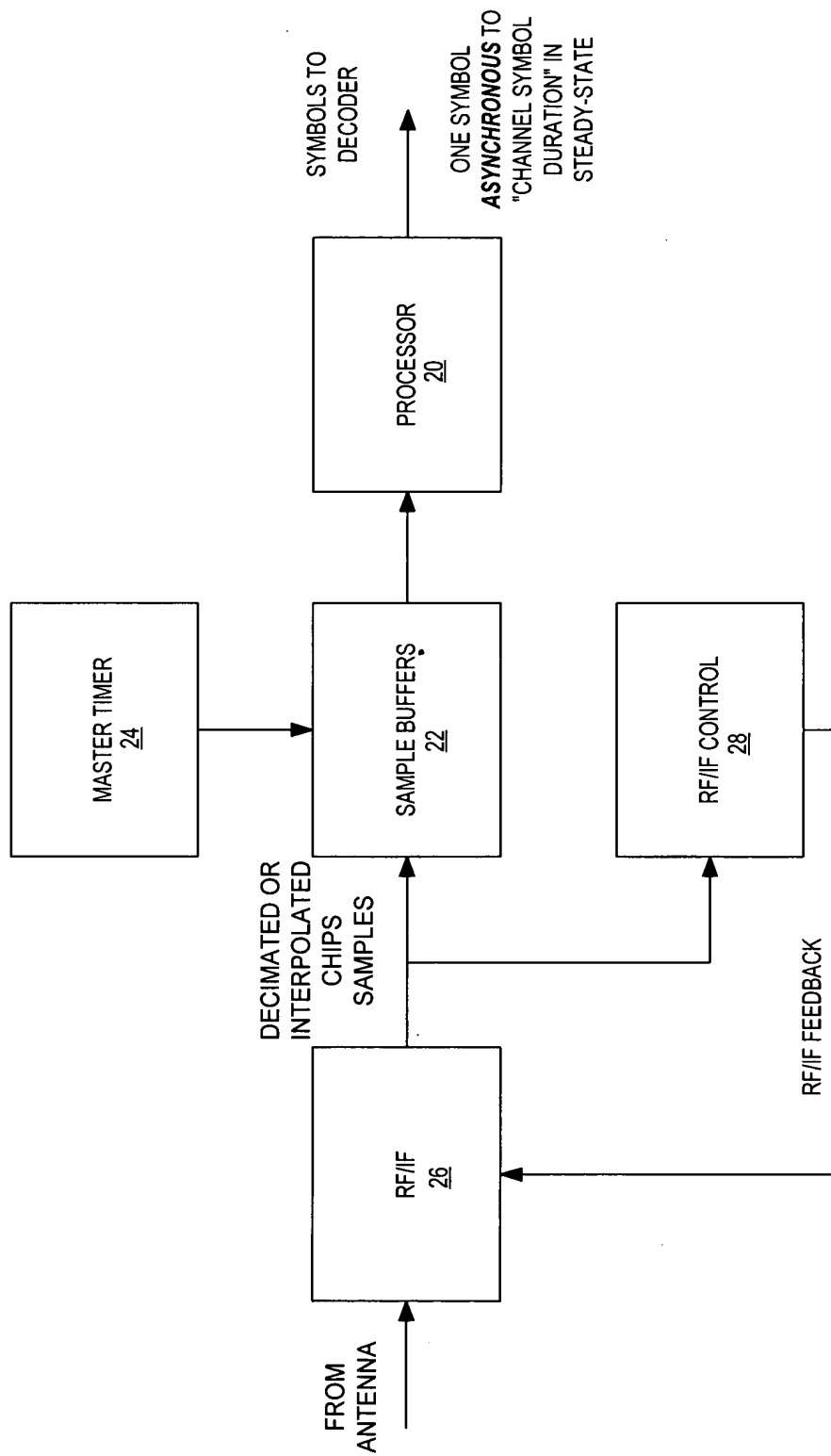
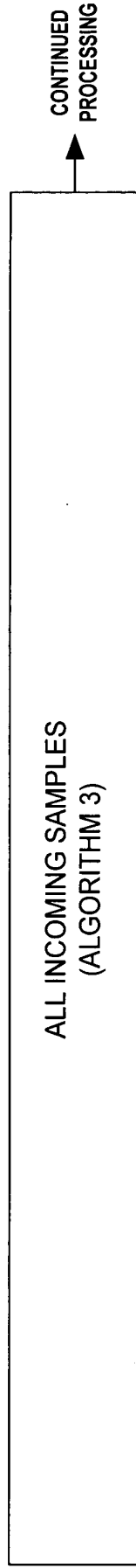


FIG. 2



CONVENTIONAL PROCESSING



OPERATION OF PROCESSOR 20

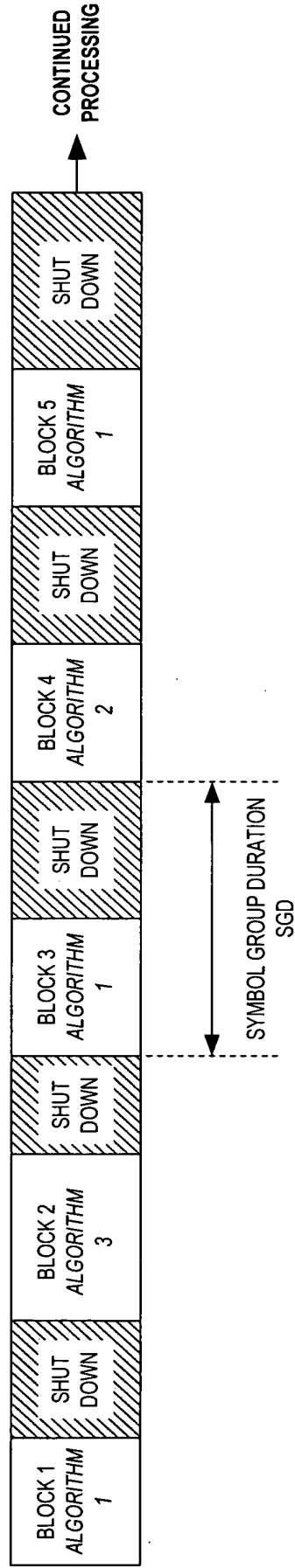
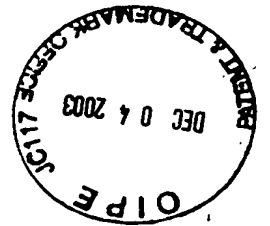
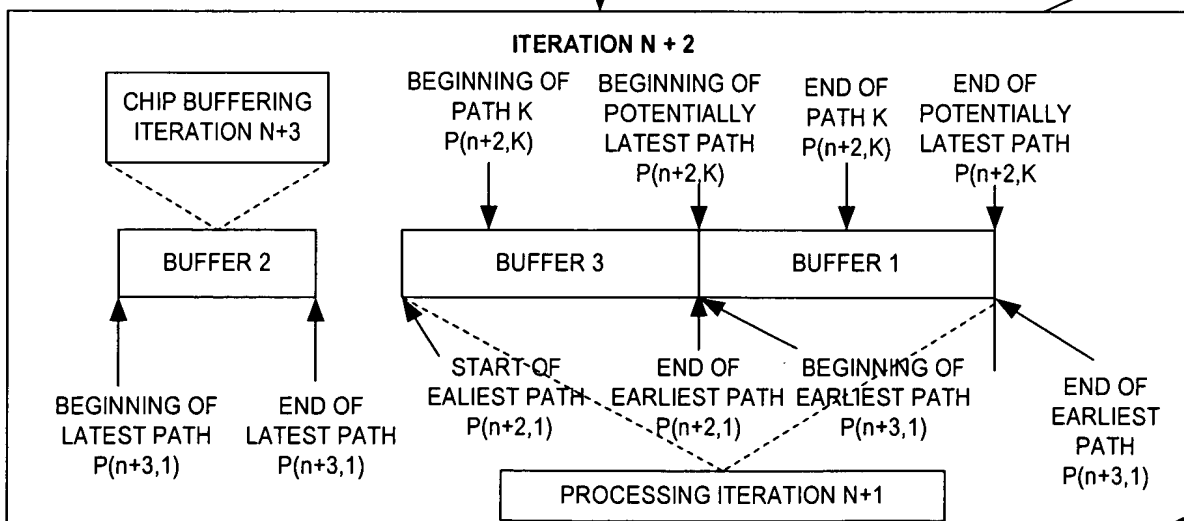
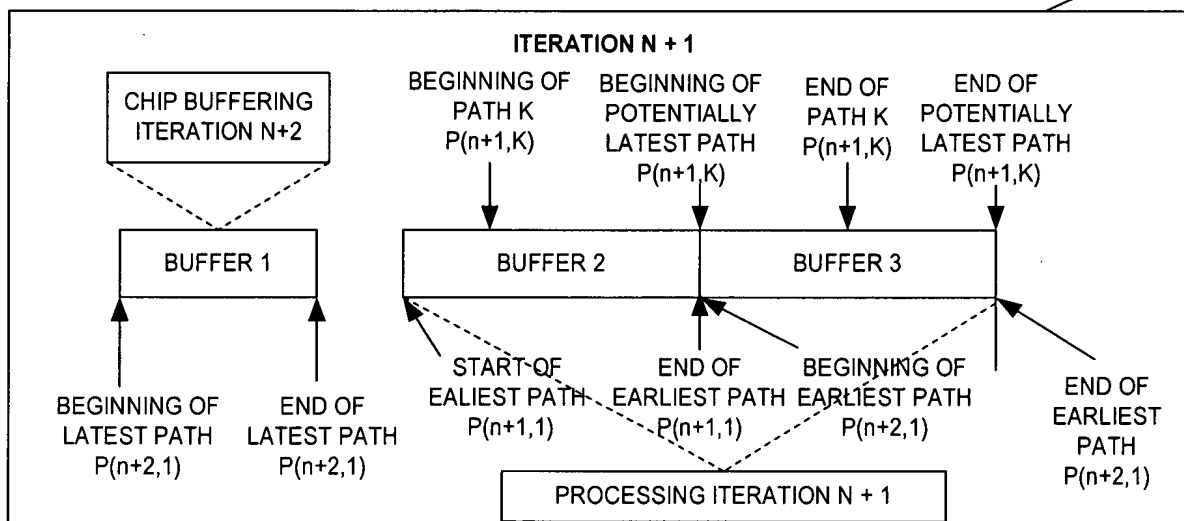
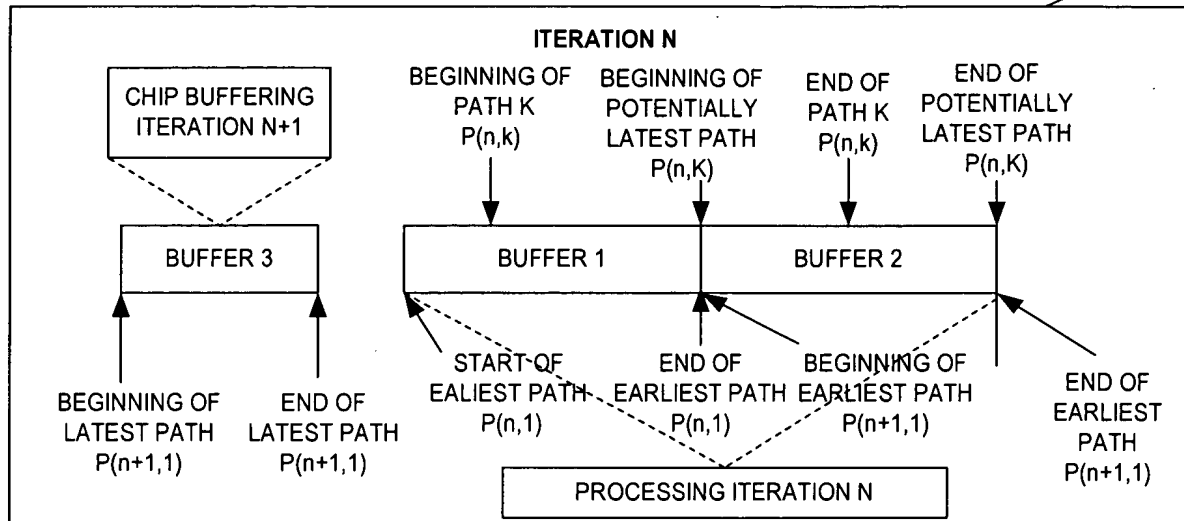


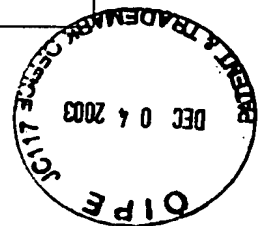
FIG. 3





N=N+3

FIG. 4



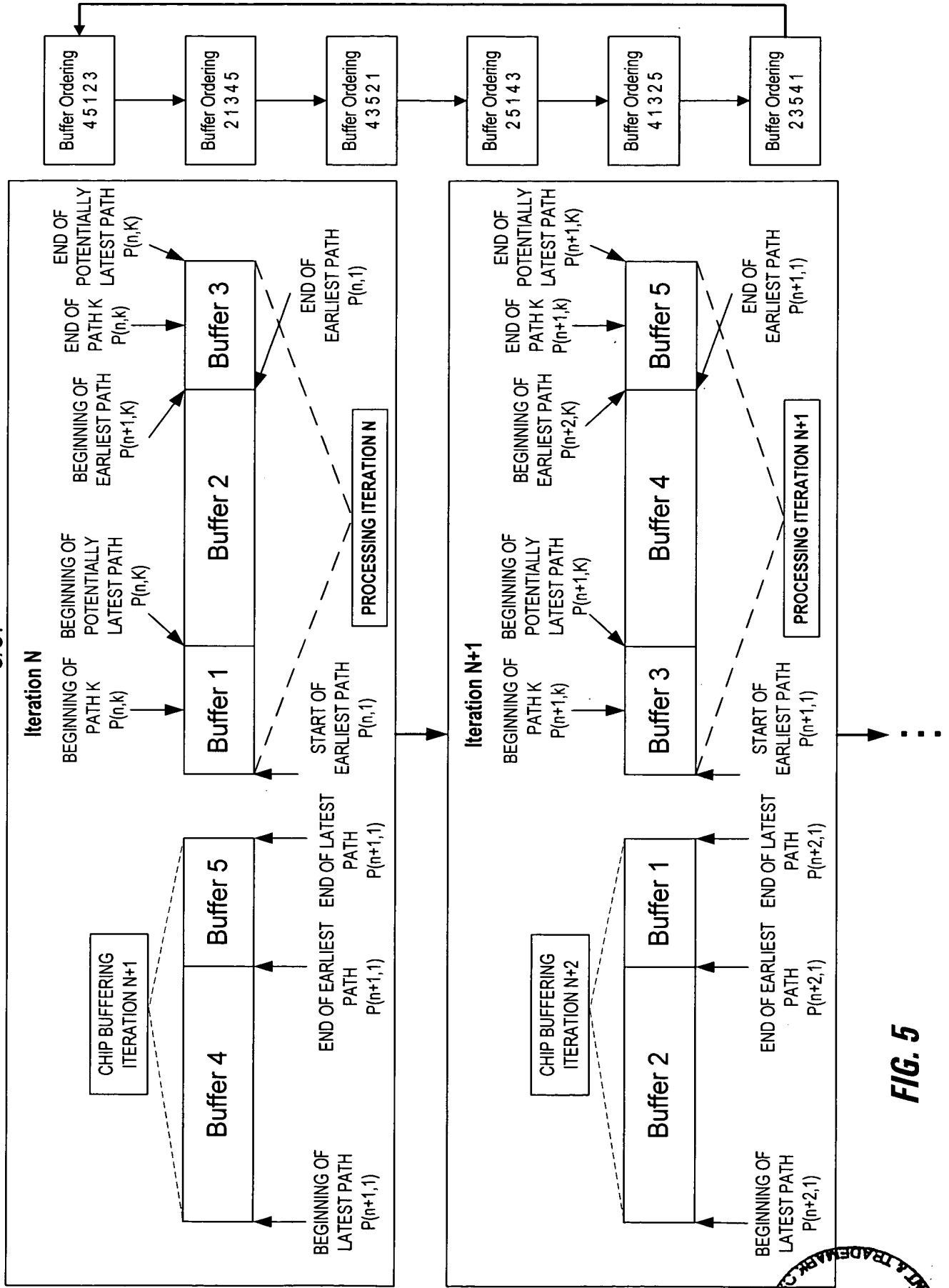


FIG. 5



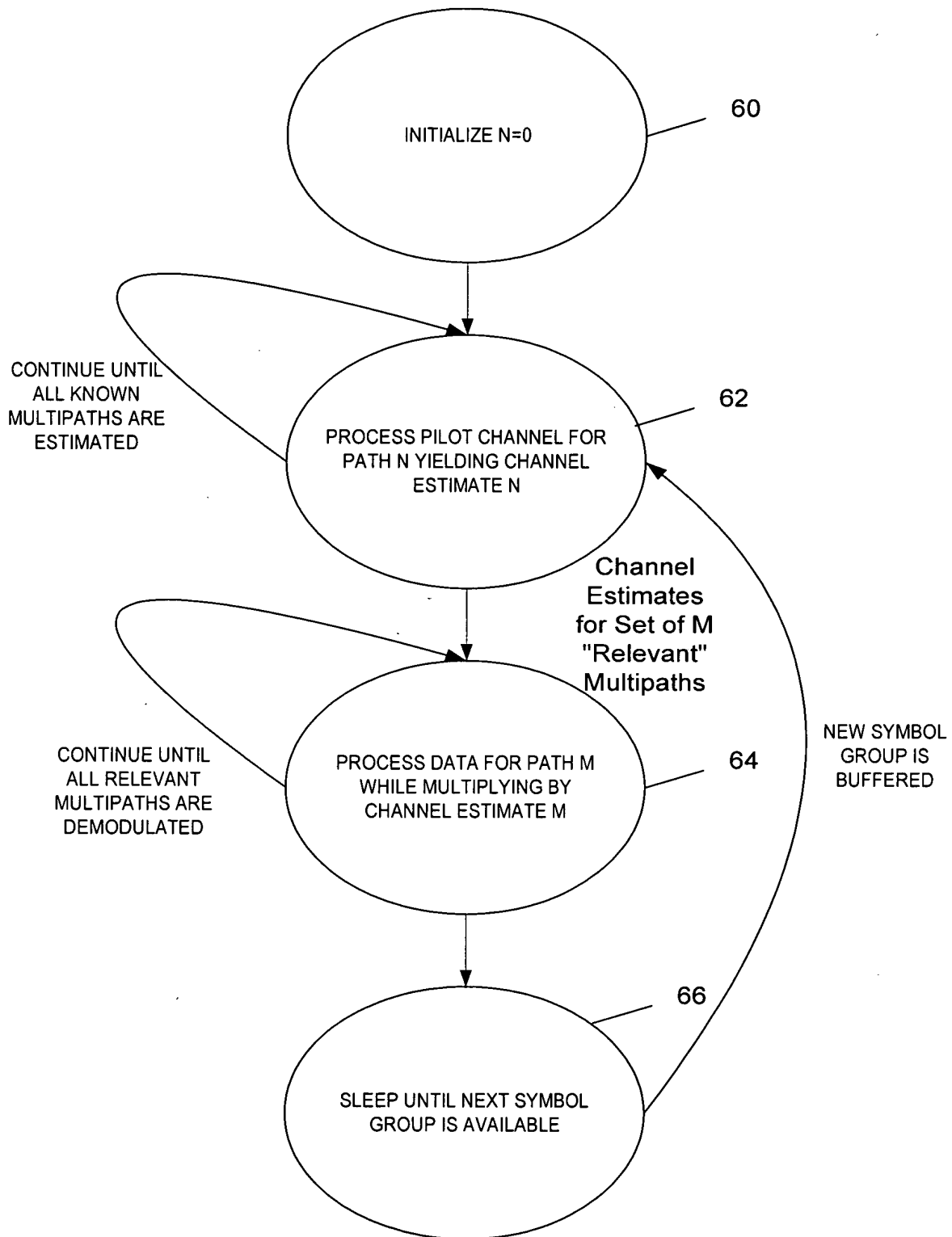
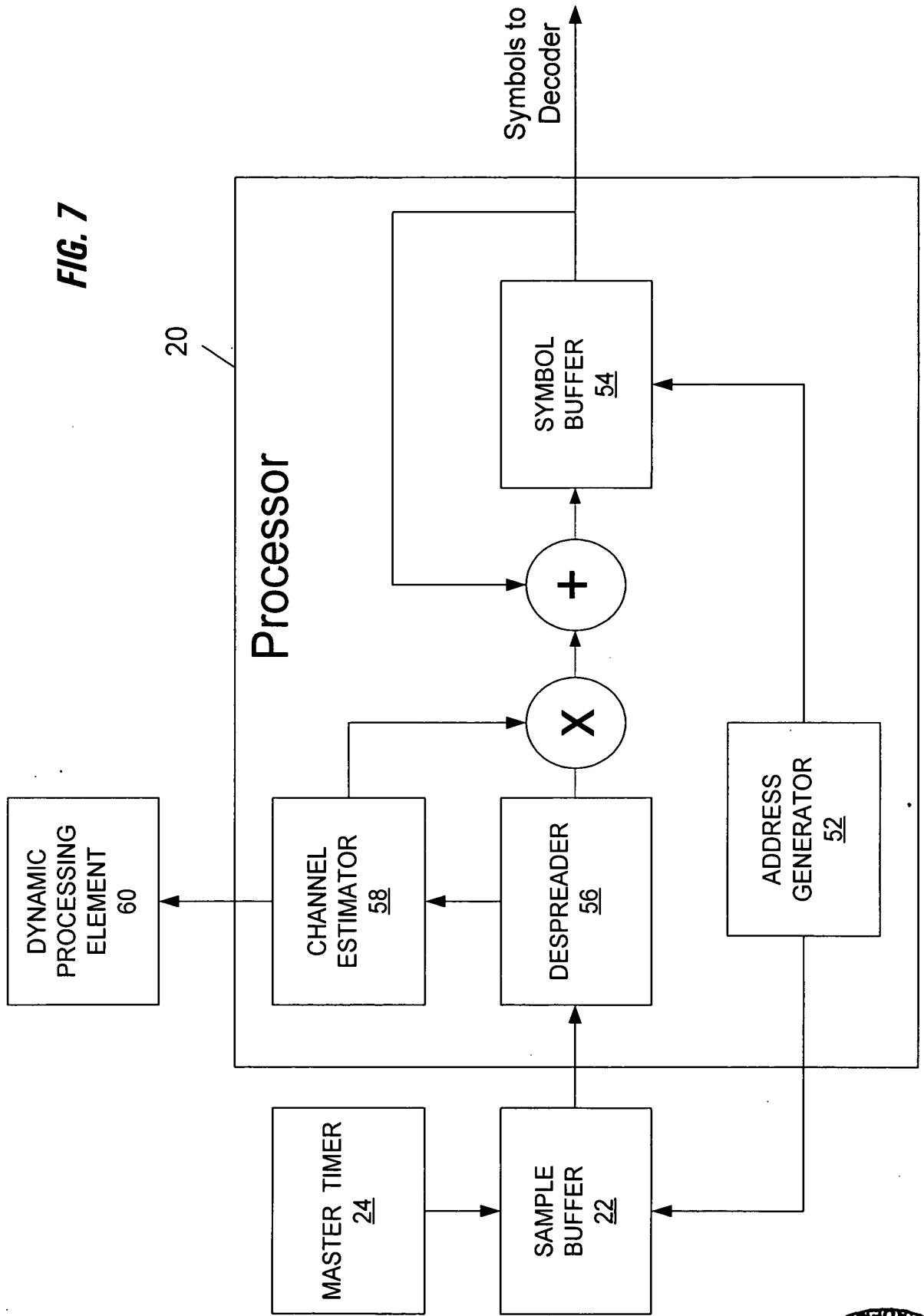
**FIG. 6**

FIG. 7



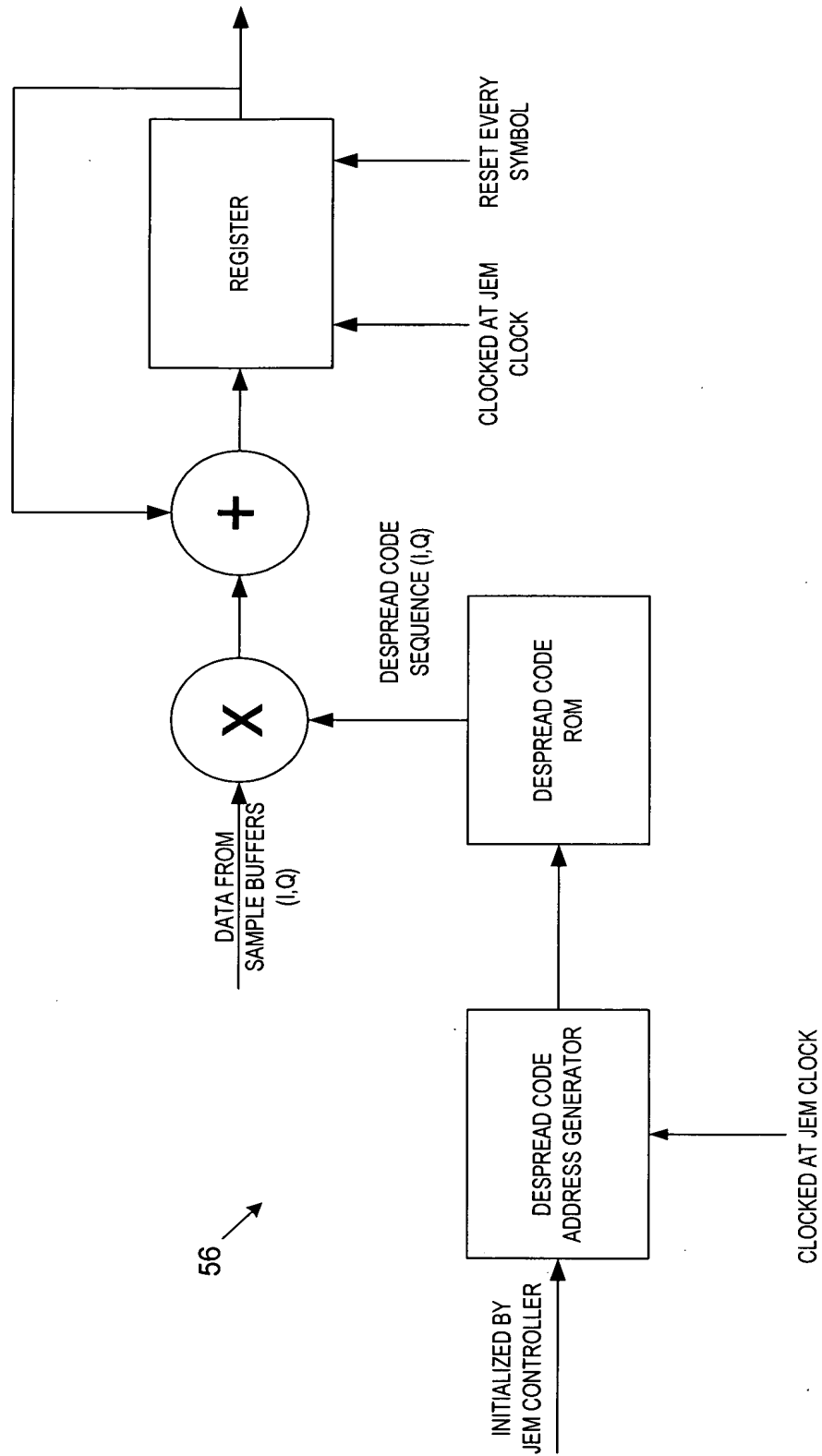
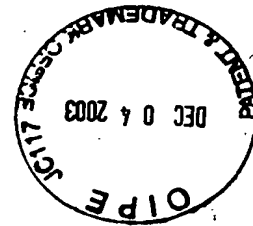


FIG. 8



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CONTINUE
UNTIL ALL N
RELEVANT
MULTIPATHS
AND
BASESTATIONS
ARE
PROCESSED

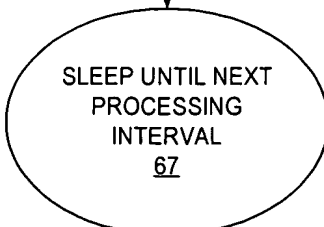
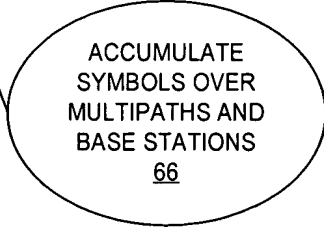
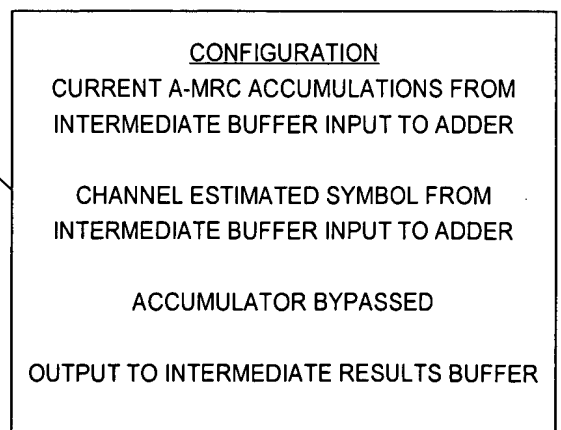
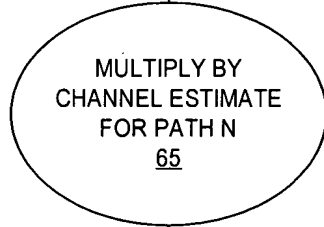
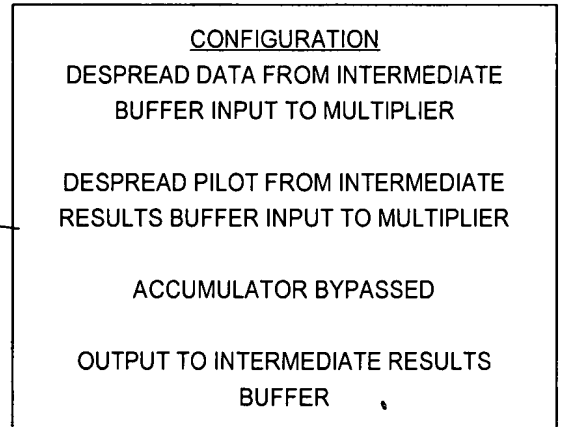
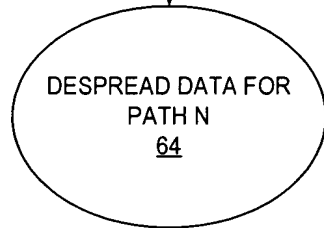
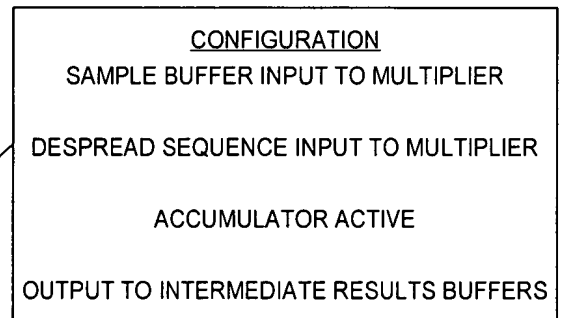
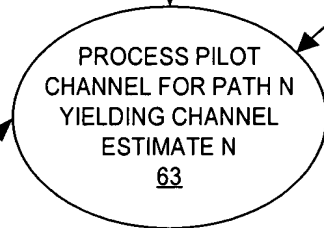
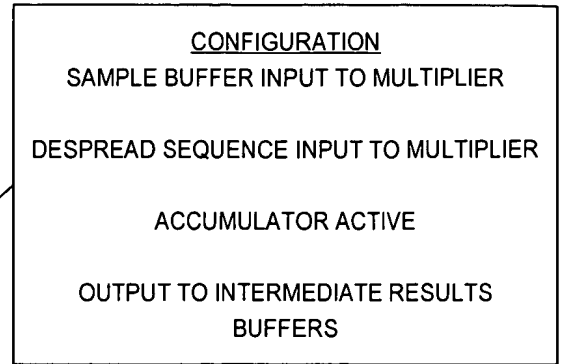
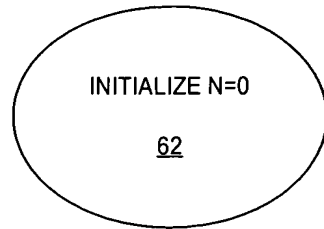
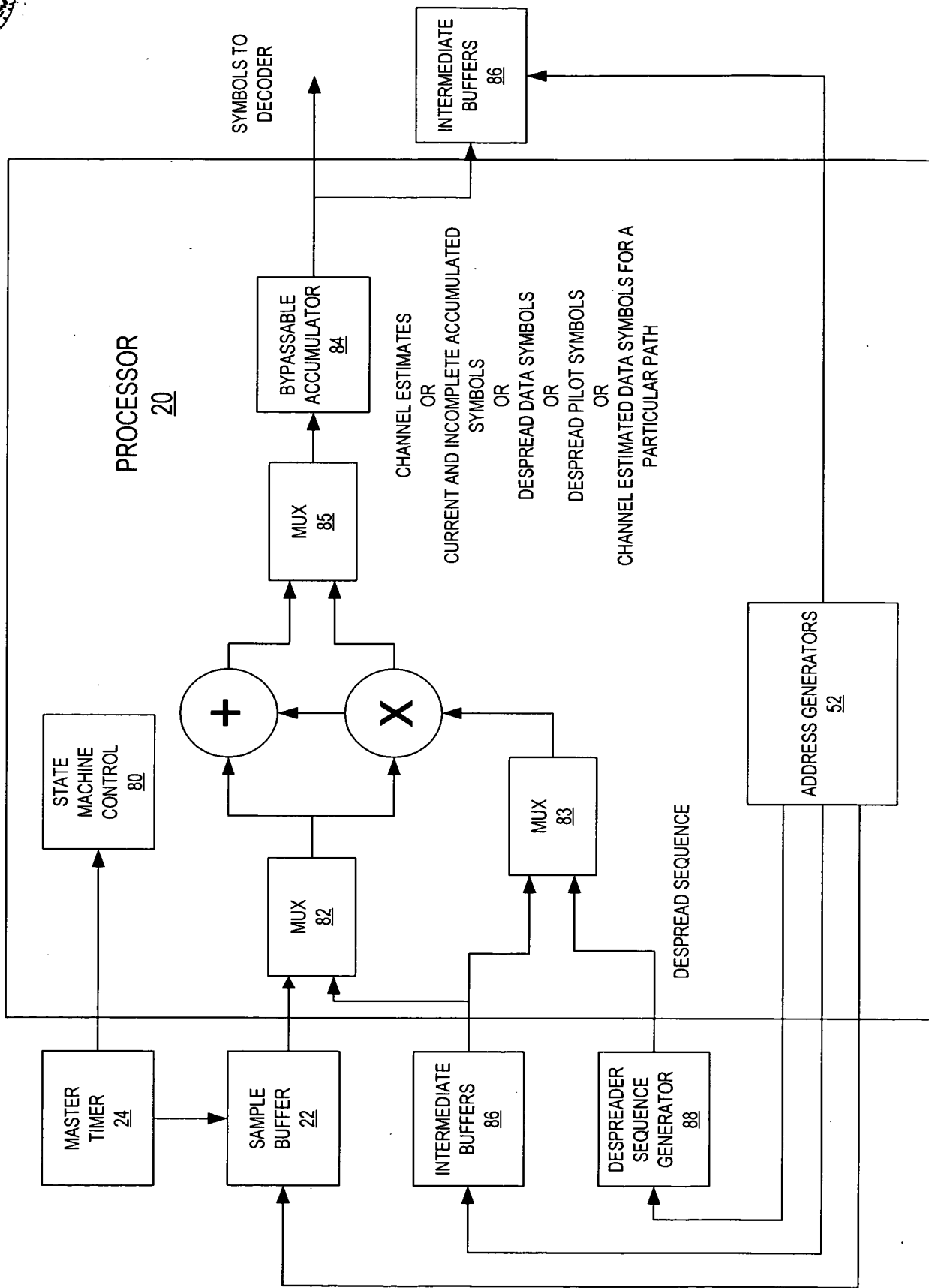


FIG. 9

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FIG. 10



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FIG. 11
PRIOR ART

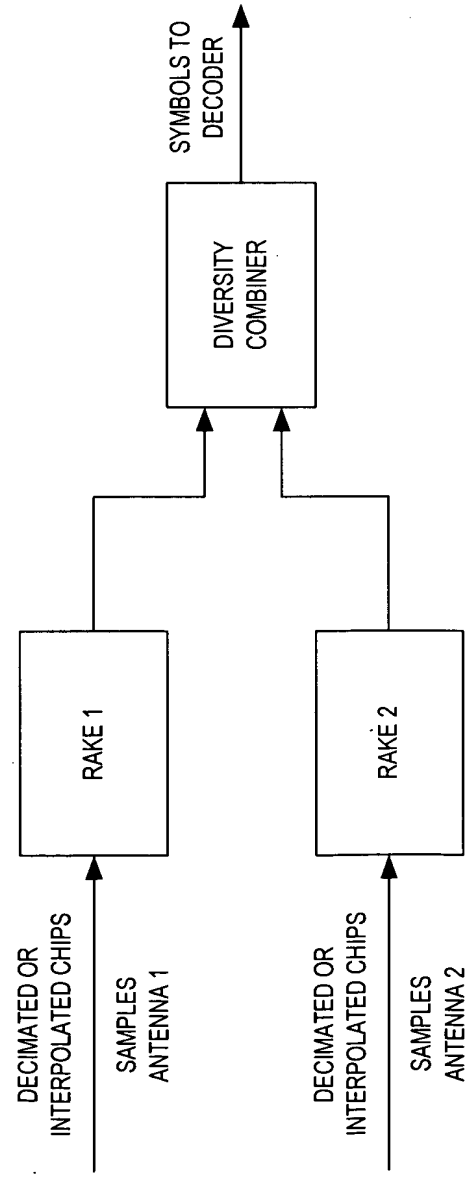
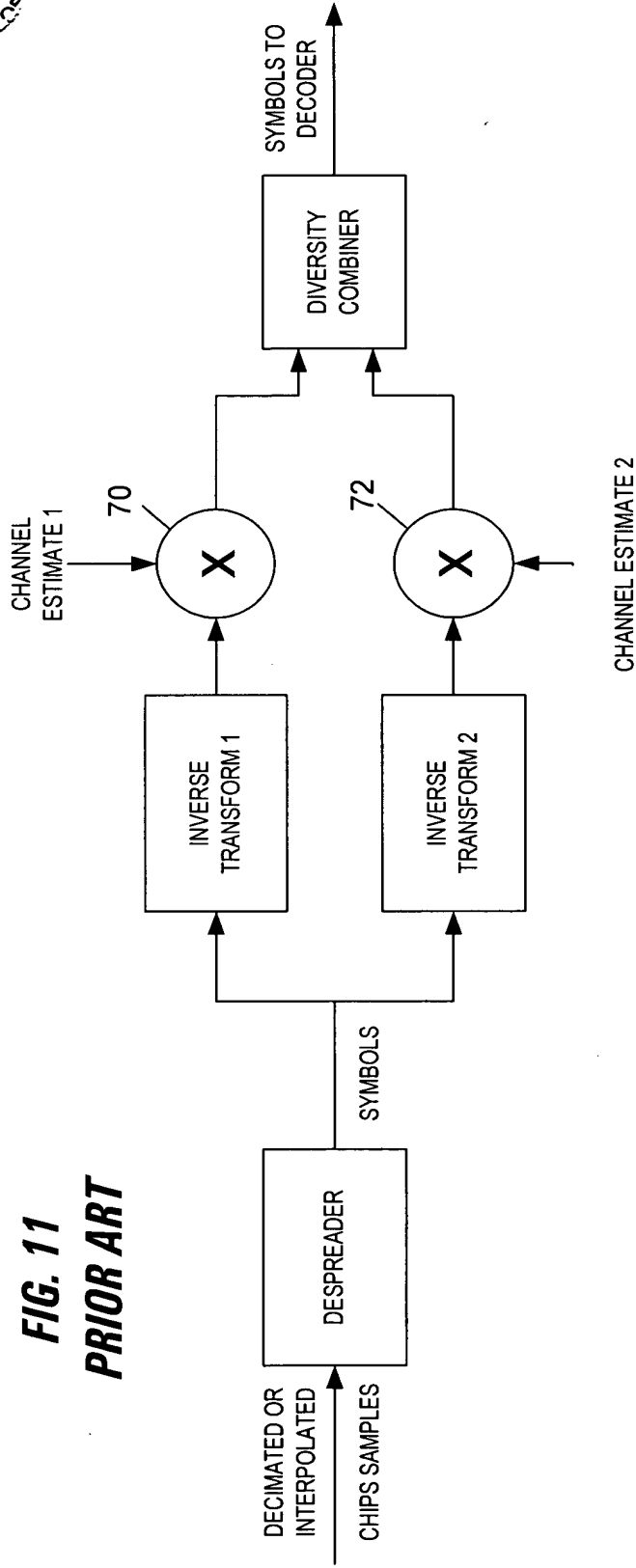


FIG. 12
PRIOR ART

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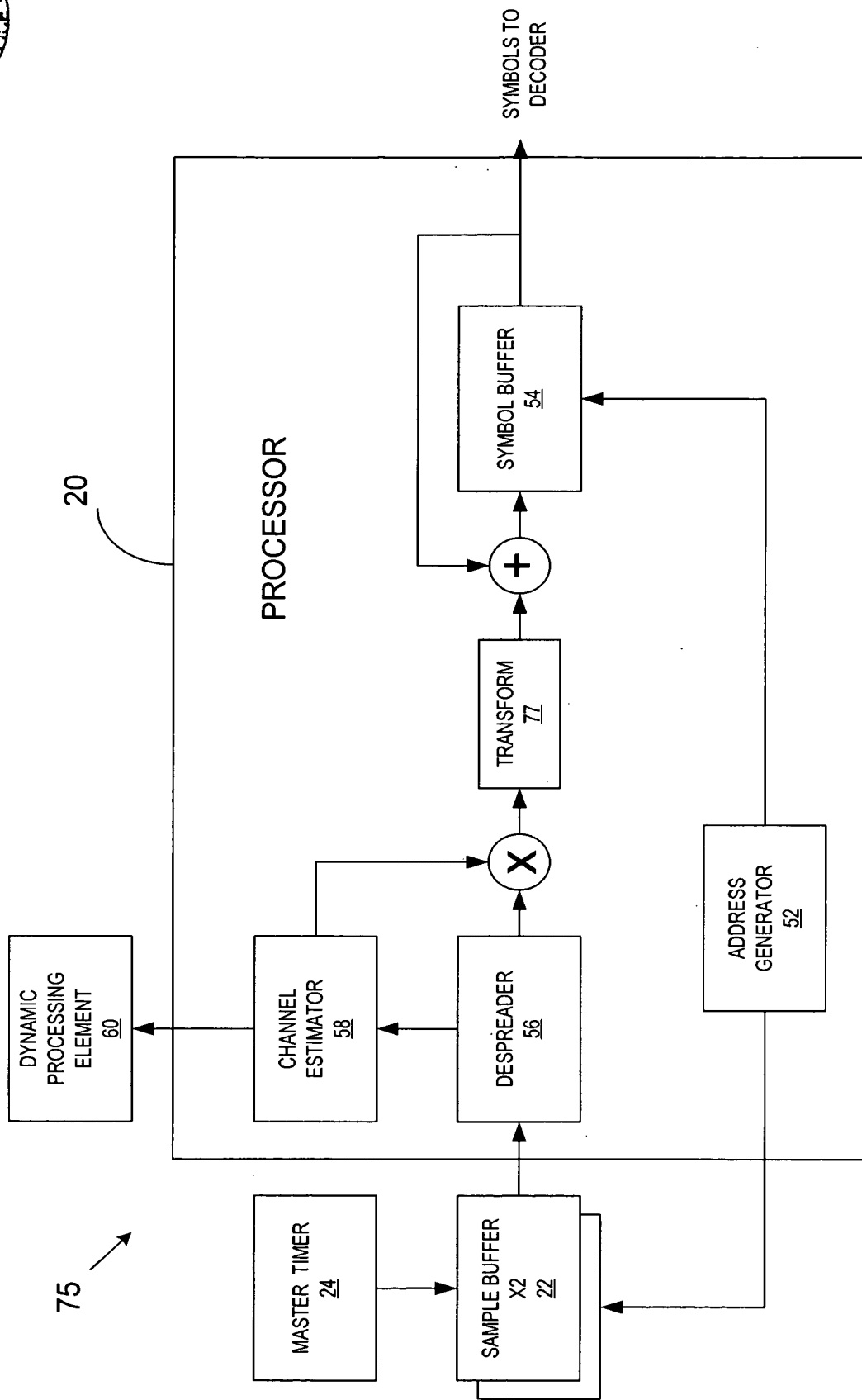


FIG. 13

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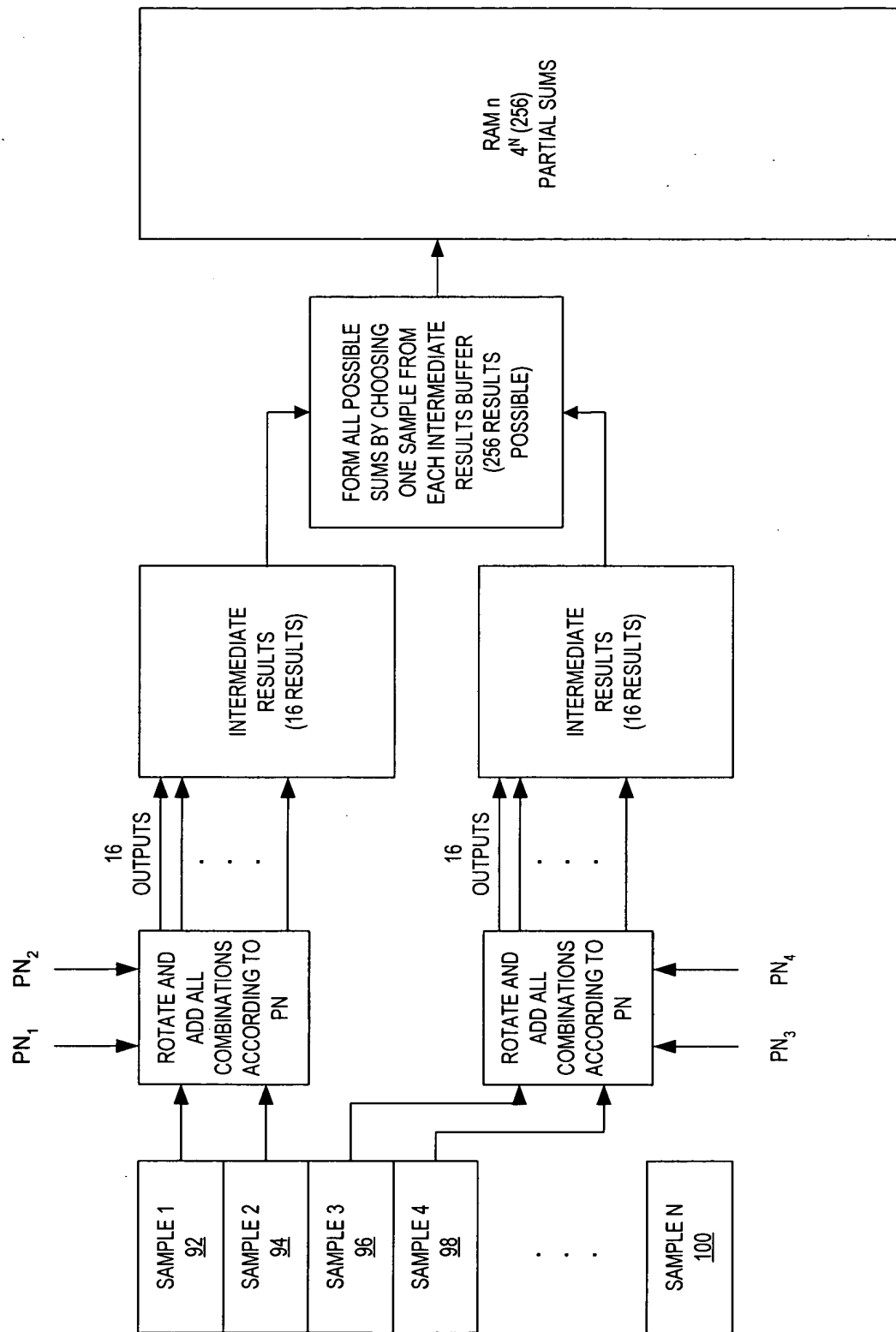


FIG. 14



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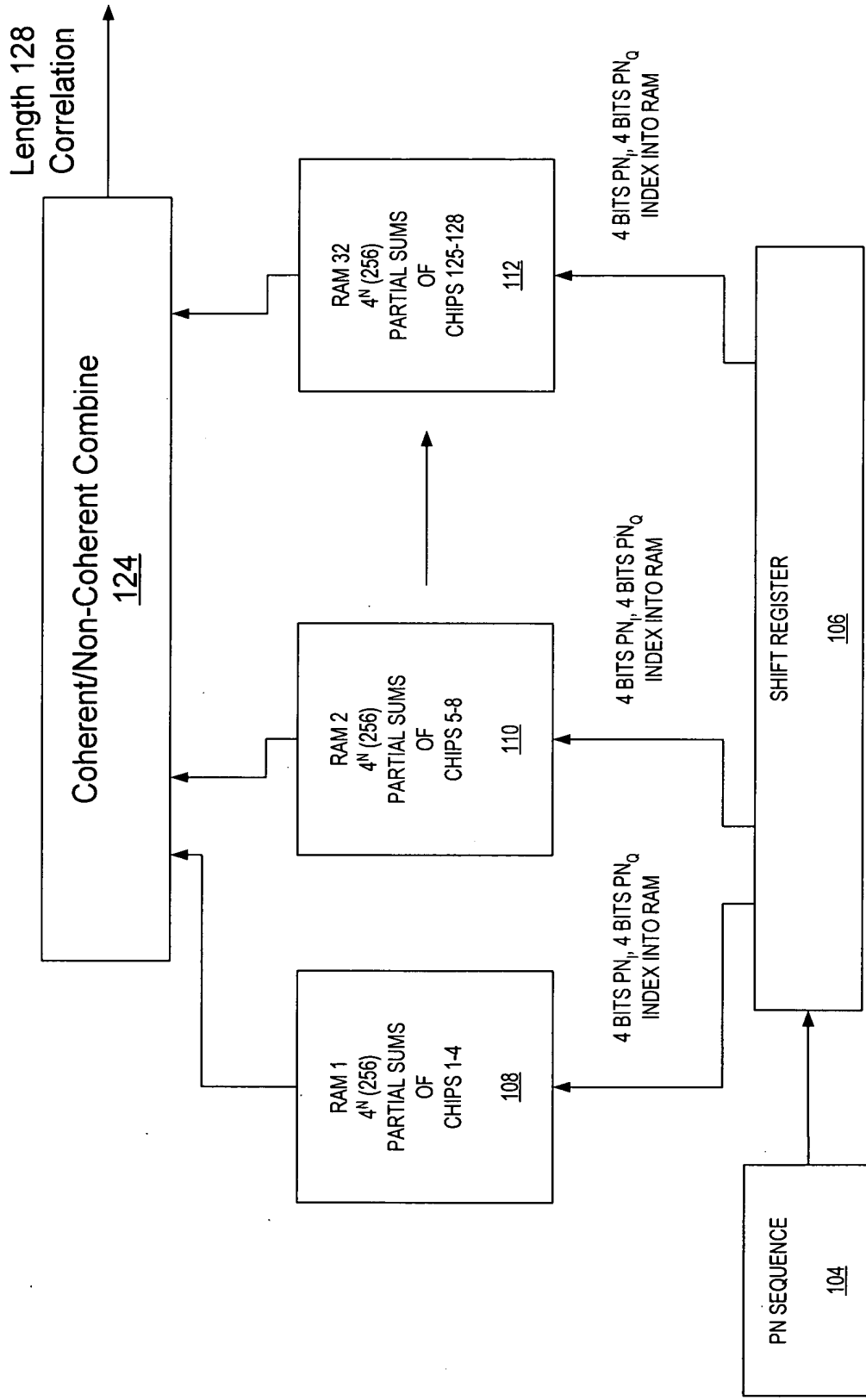


FIG. 15

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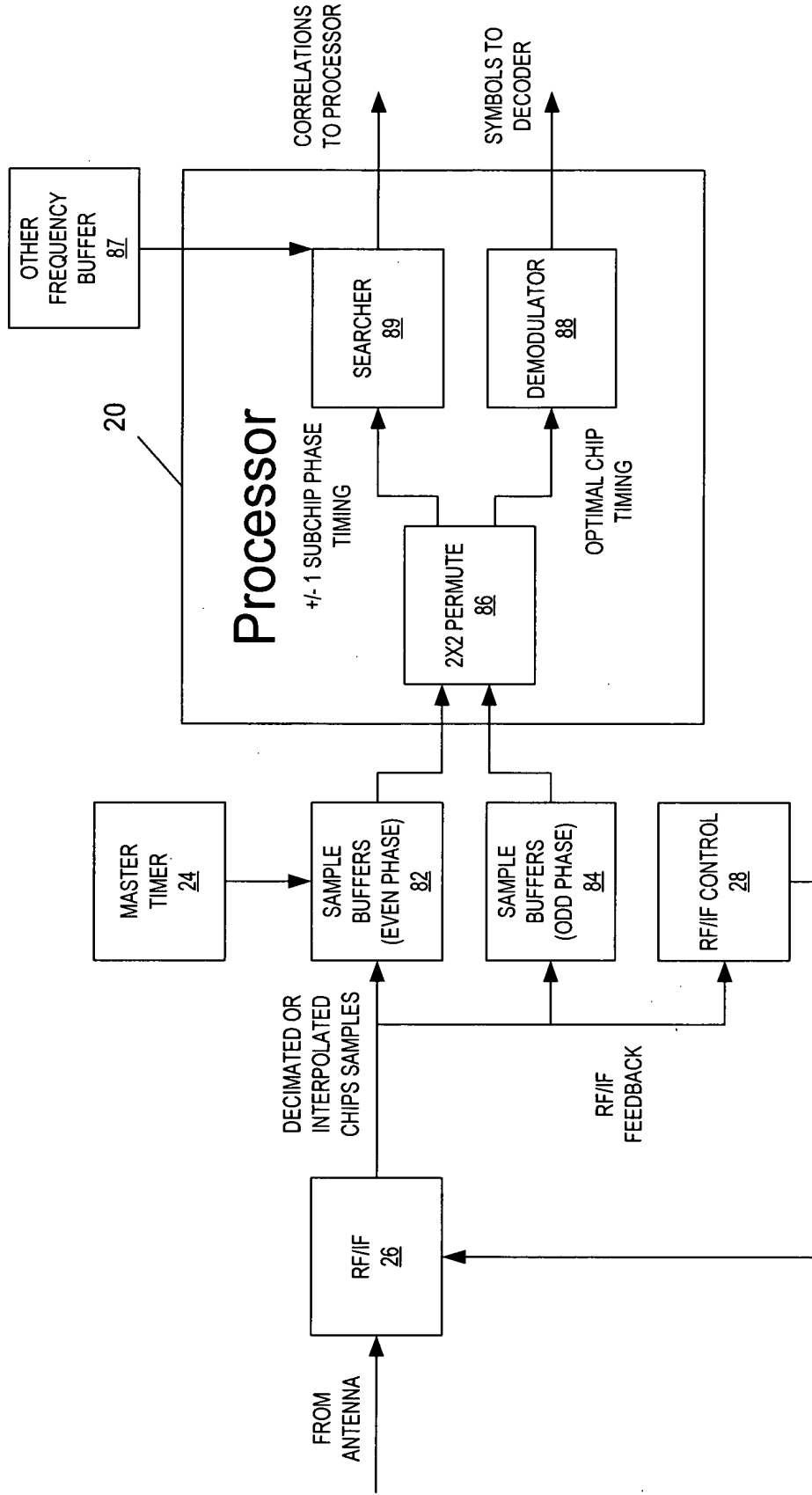
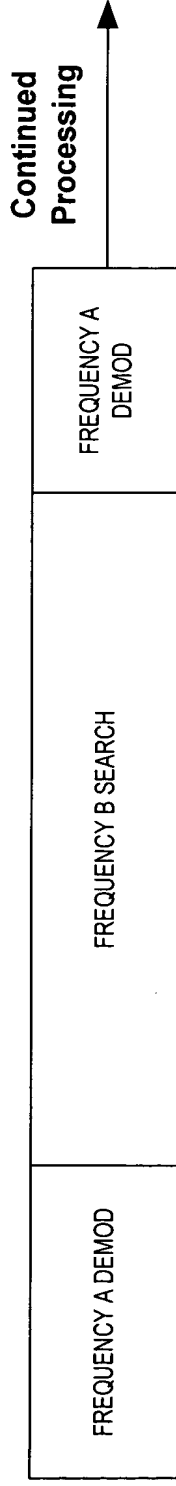


FIG. 16



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CONVENTIONAL PROCESSING



MULTI-FREQUENCY PROCESSING

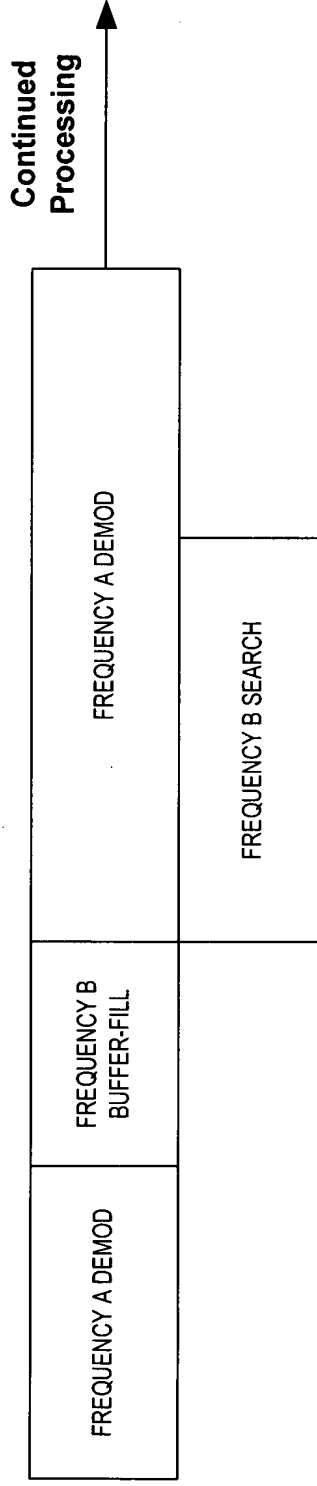


FIG. 17

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$$R = 4 \left(\frac{E_c}{N_o} \right) \left[\frac{1}{\sqrt{E_c}} \right]$$

Received Chip, r_n

Convergent Searcher

MULTI BY CHAN
RELIABILITY, R

S_{chan}

S_n

S_{n-1} S_{n-2} S_{n-3} S_{n-4} S_{n-5} S_{n-6} S_{n-7} S_{n-8} S_{n-9} S_{n-10} S_{n-11} S_{n-12} S_{n-13} S_{n-14} S_{n-15}

SOFT COMBINER
(MOD 2 ADDITION)

$S_{SOFT-PN}$

FIG. 18

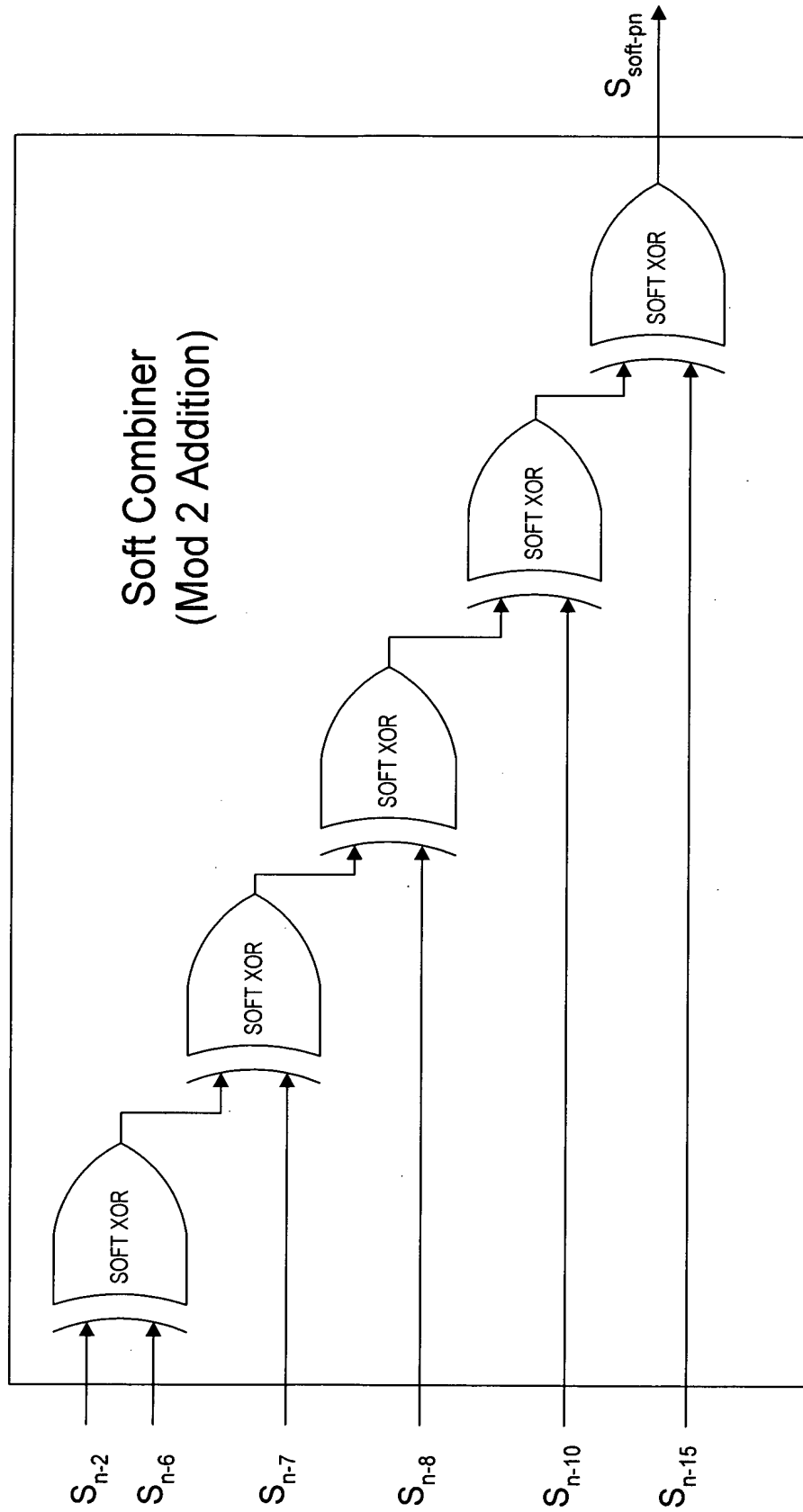


FIG. 19

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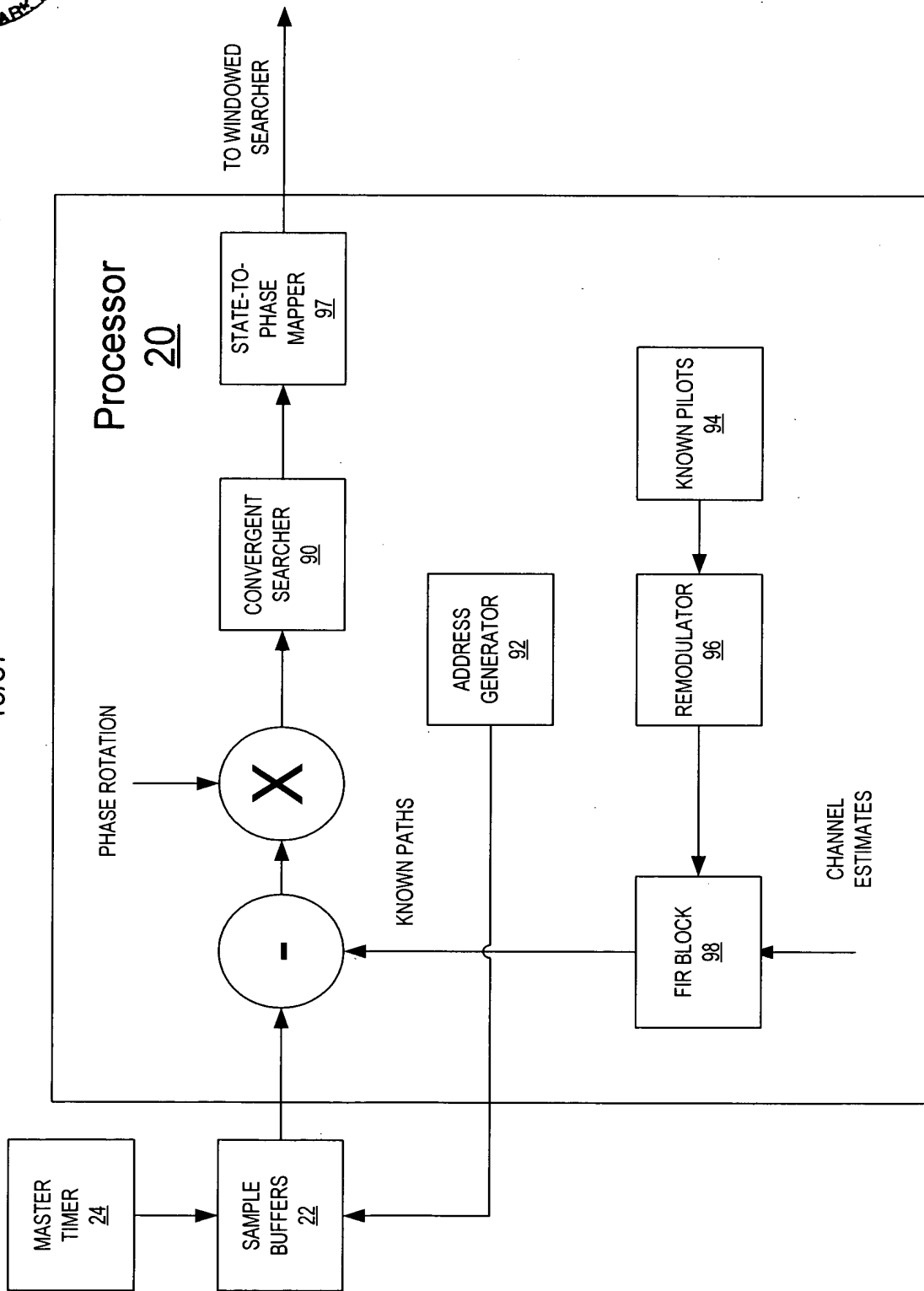
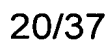


FIG. 20



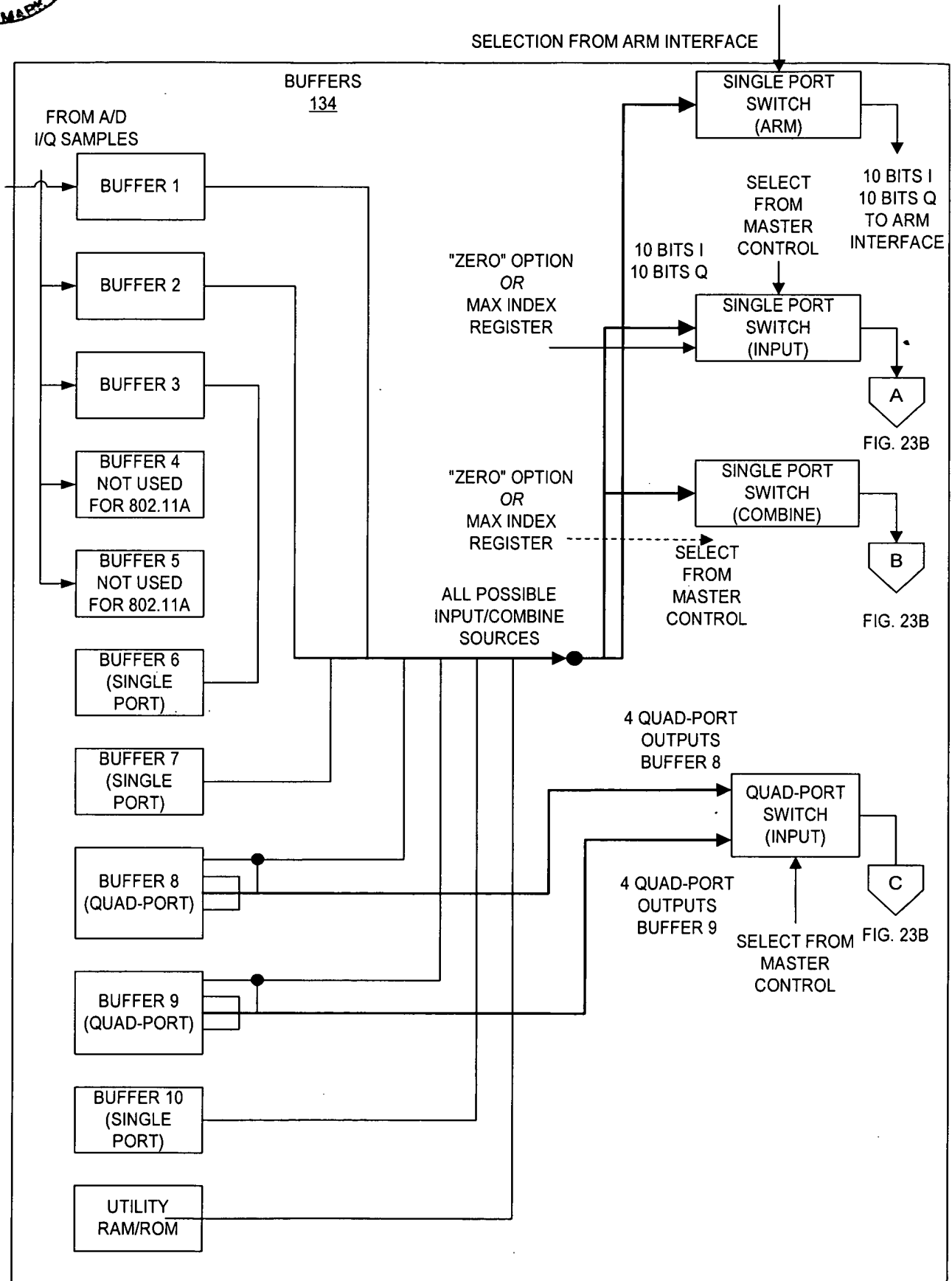
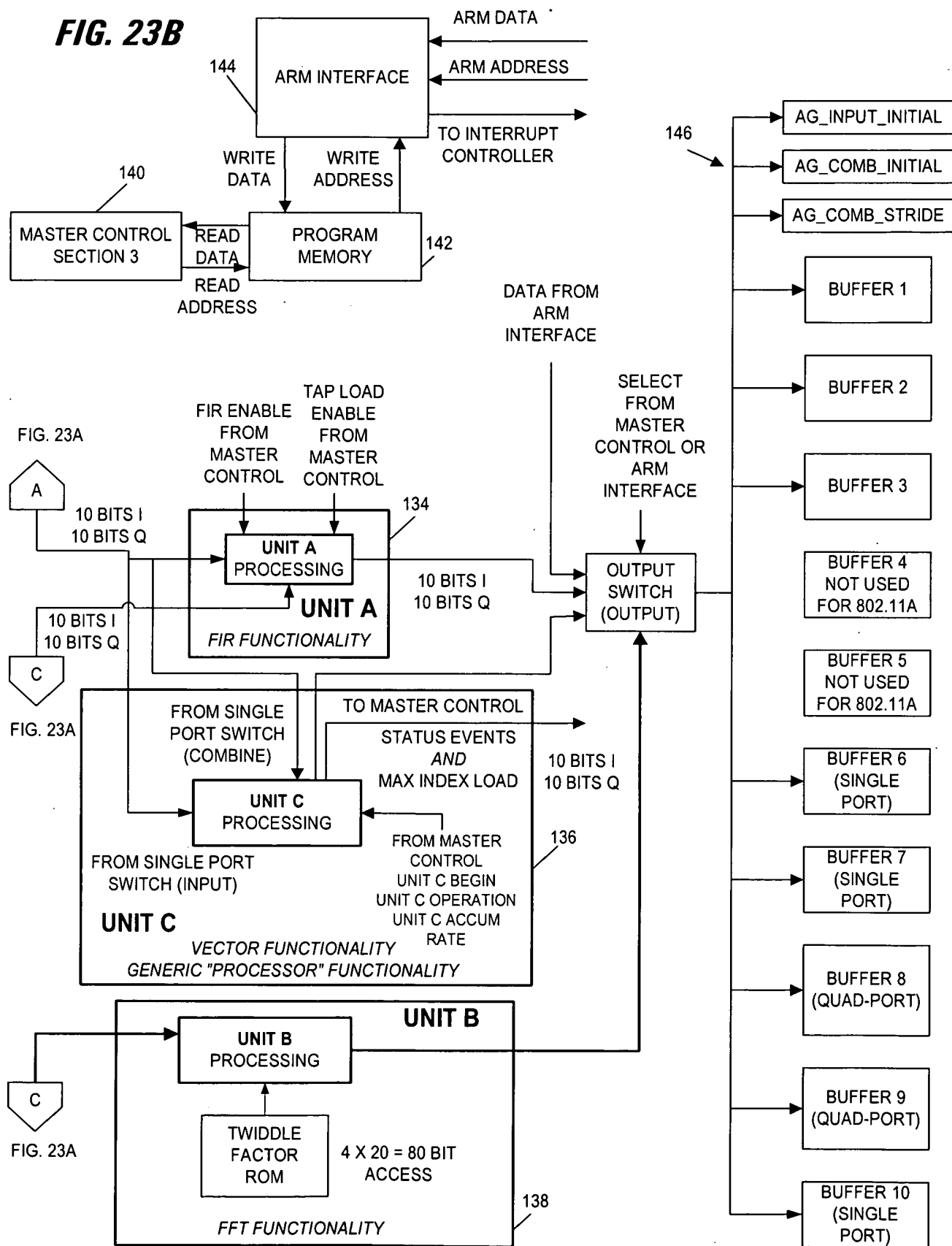
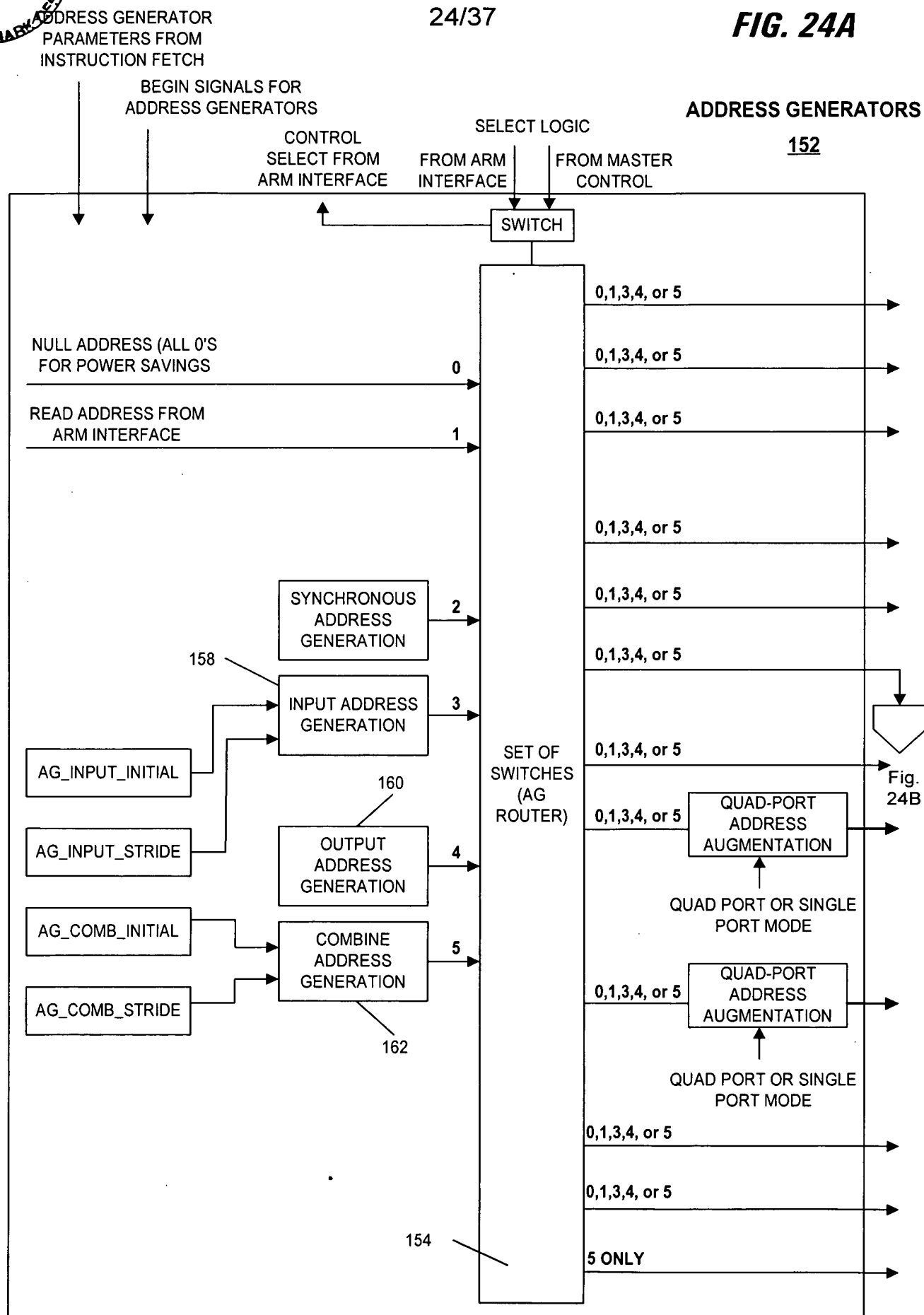


FIG. 23A

FIG. 23B





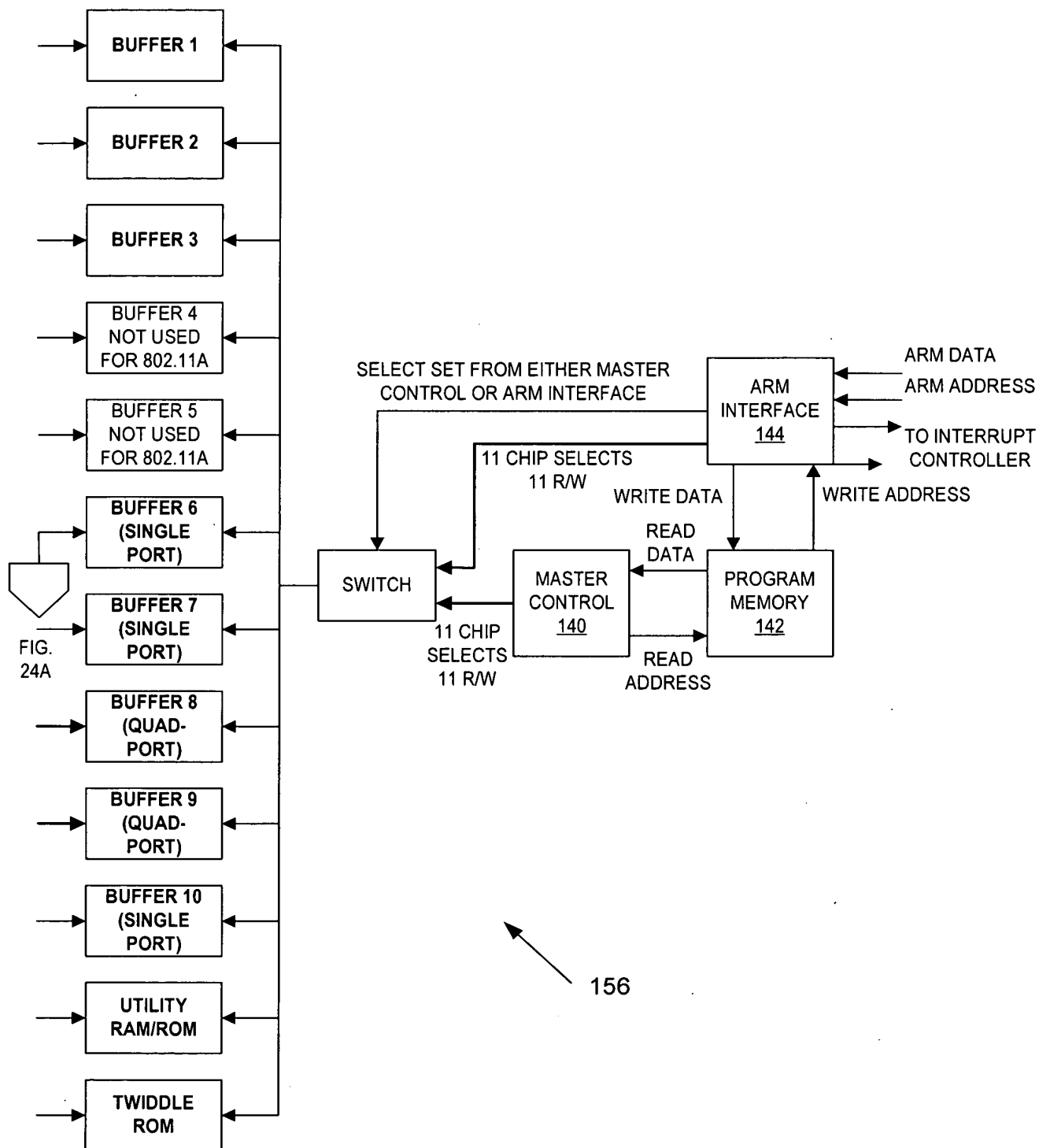
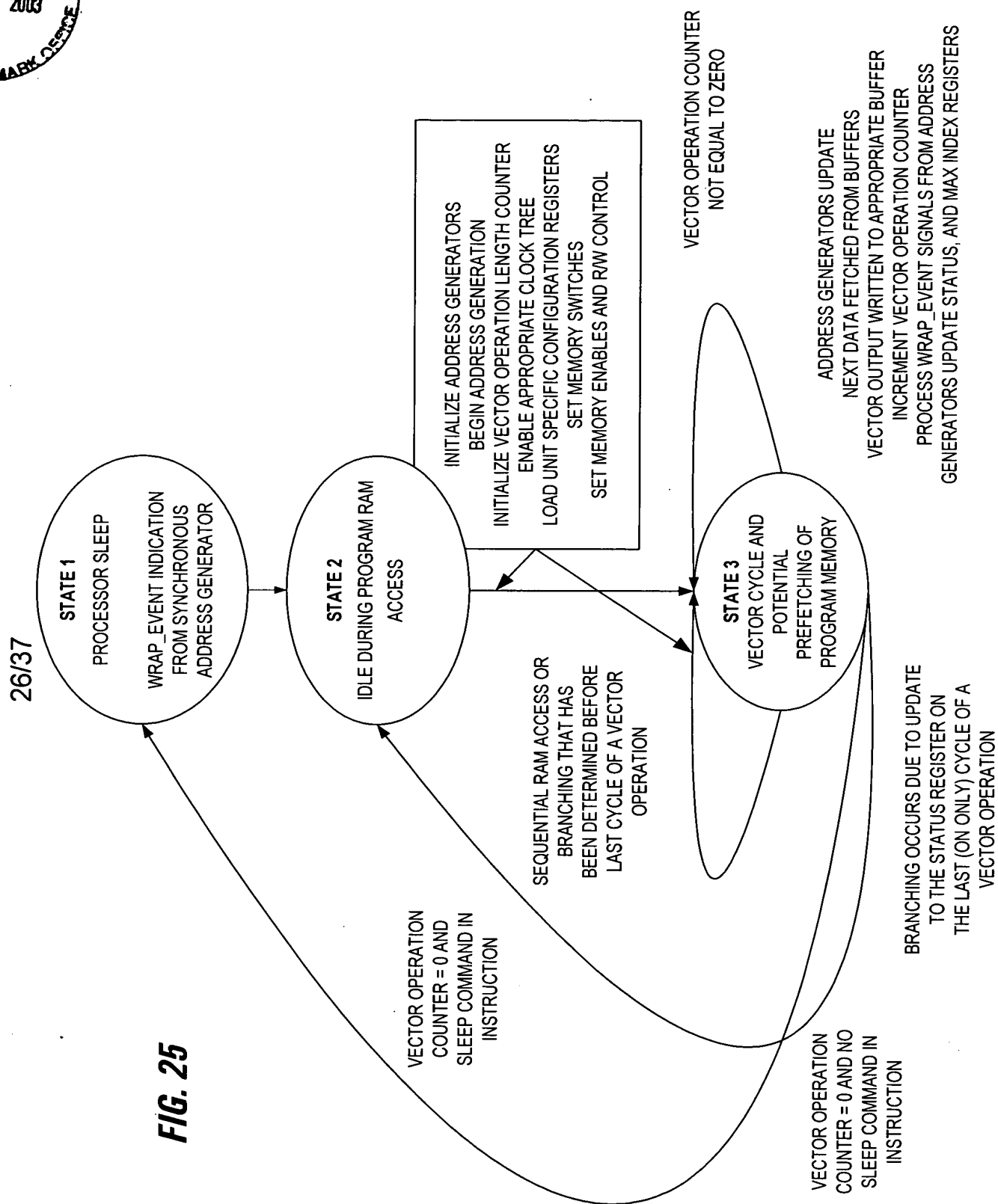


FIG. 24B

FIG. 25



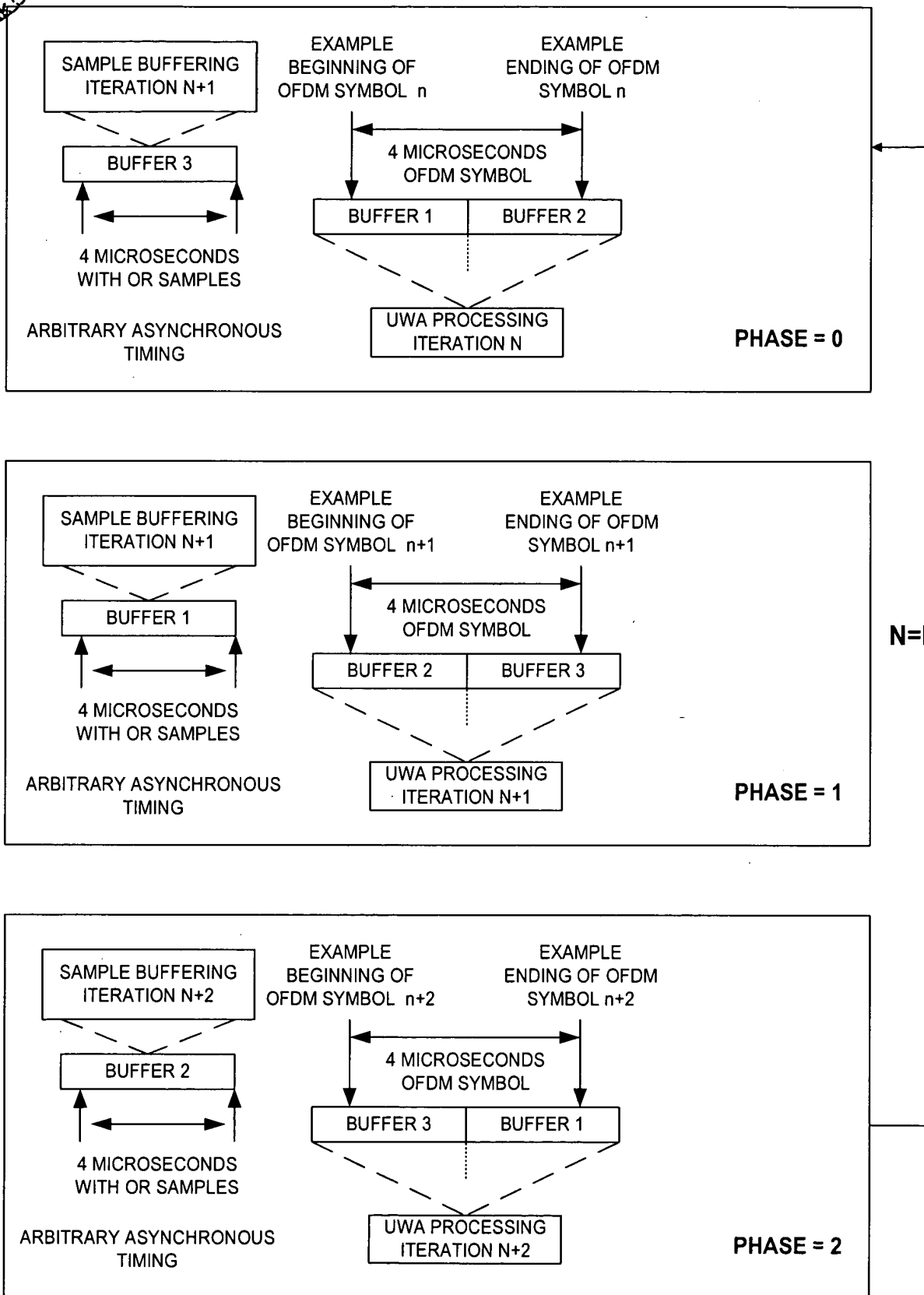
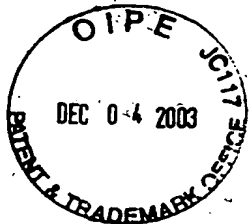
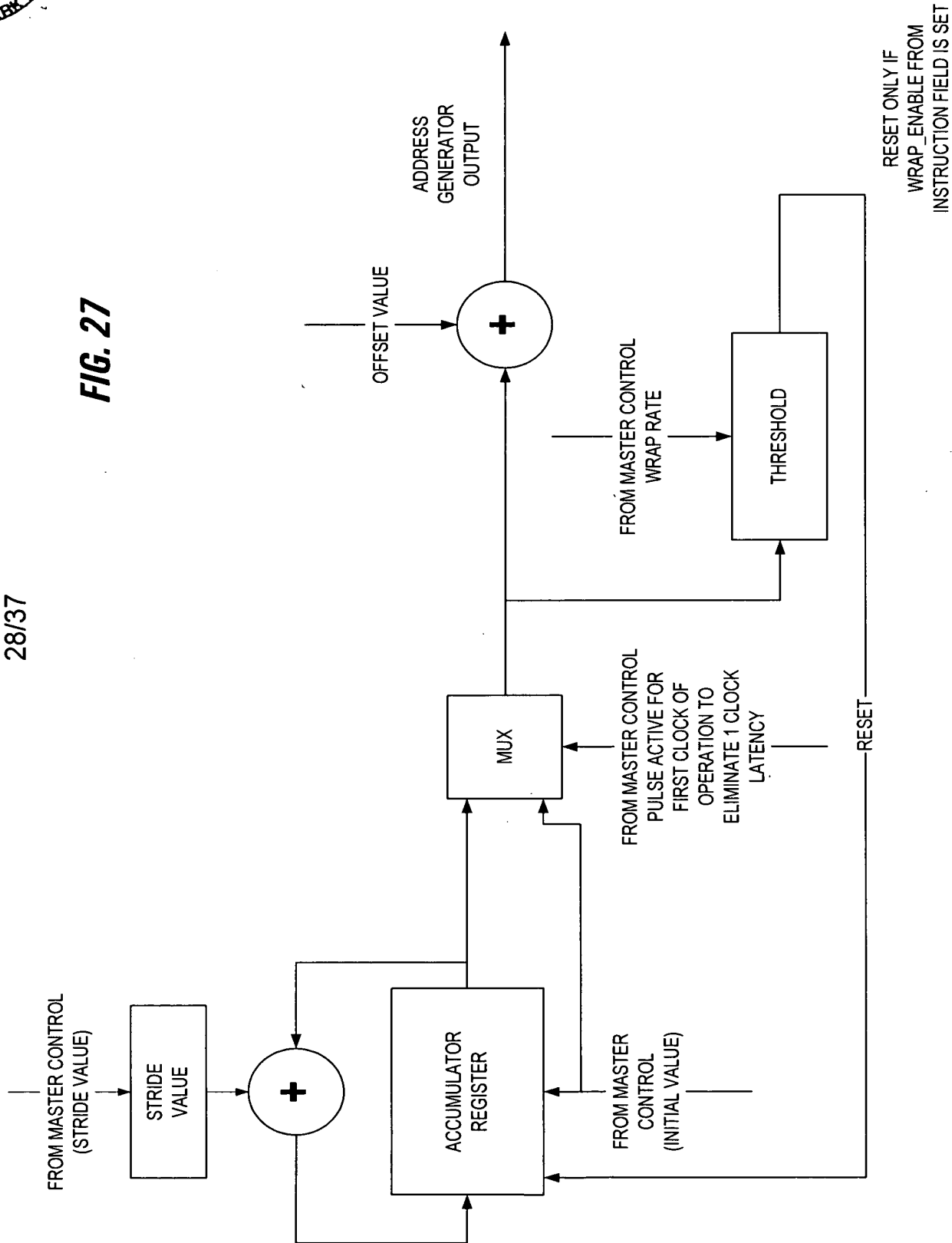


FIG. 26



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FIG. 27



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CLOCK UNDER
CONTROL OF VECTOR
STATE MACHINE

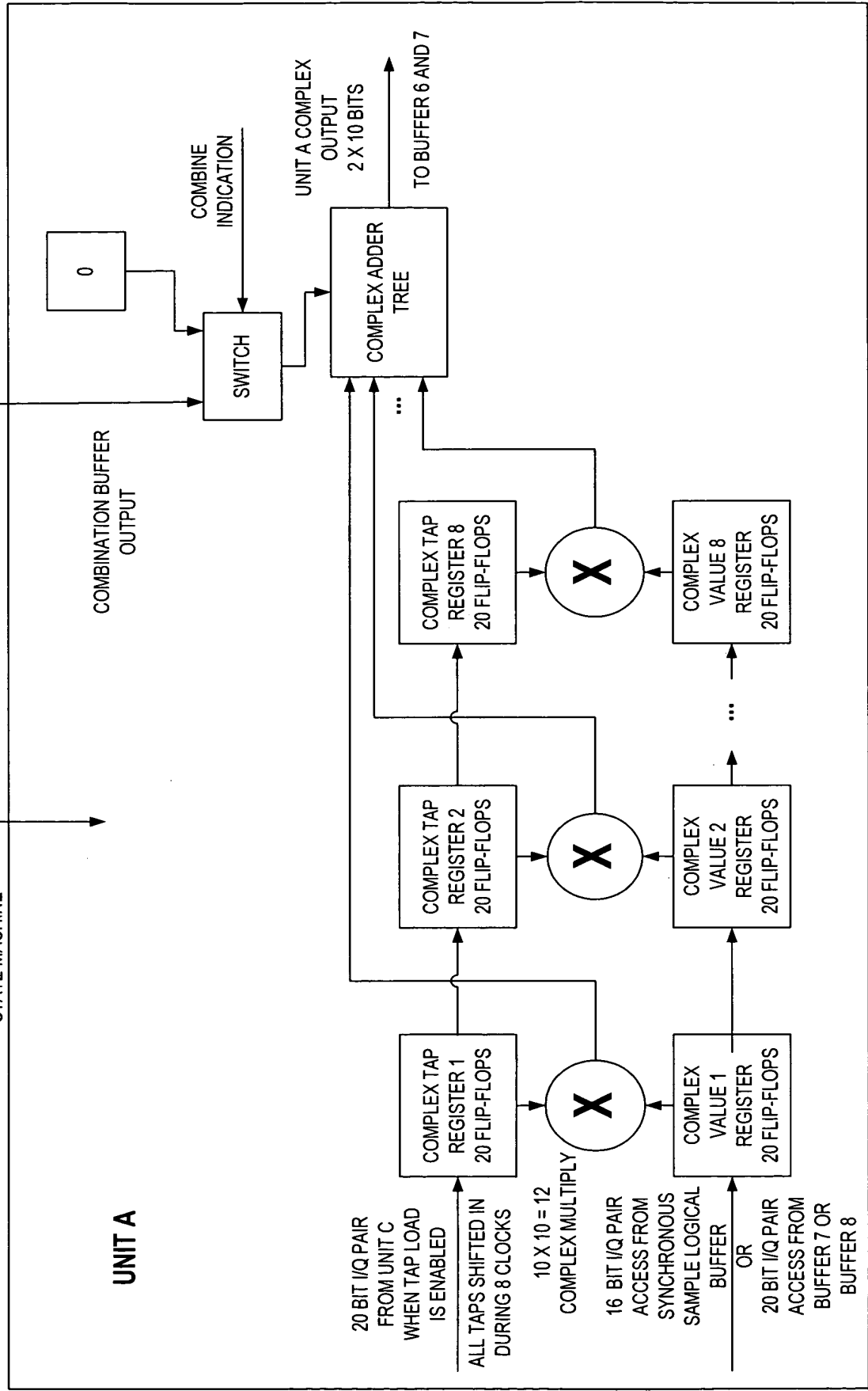


FIG. 28

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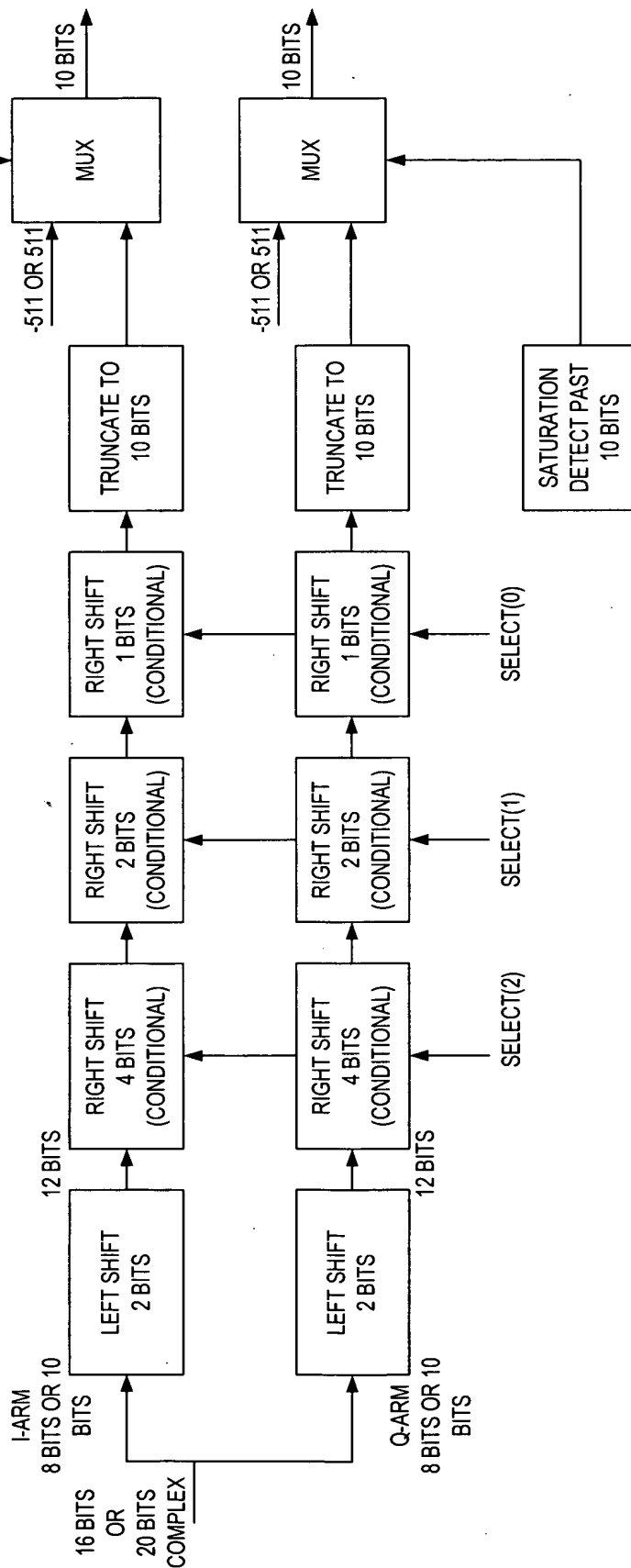


FIG. 29

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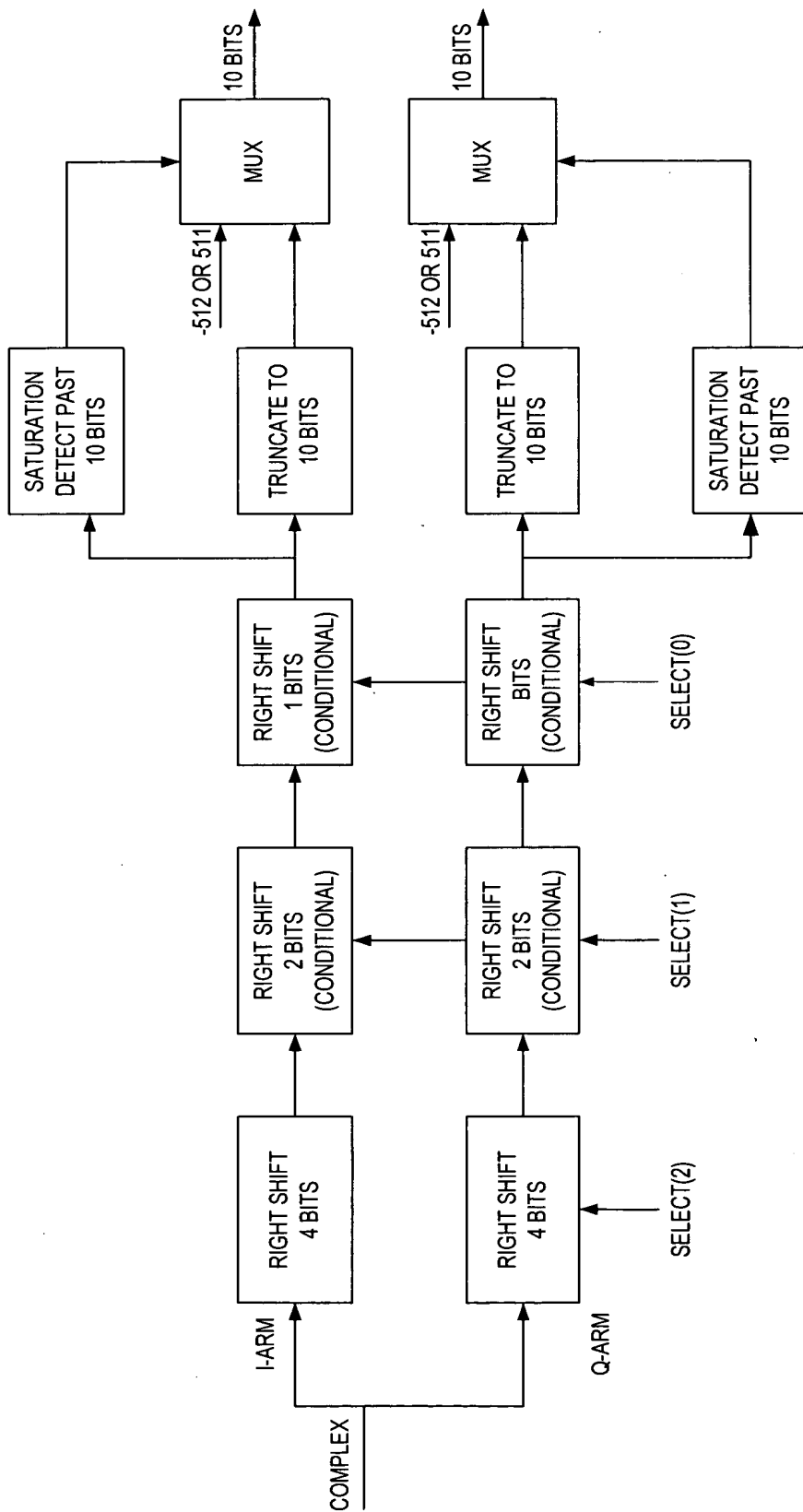
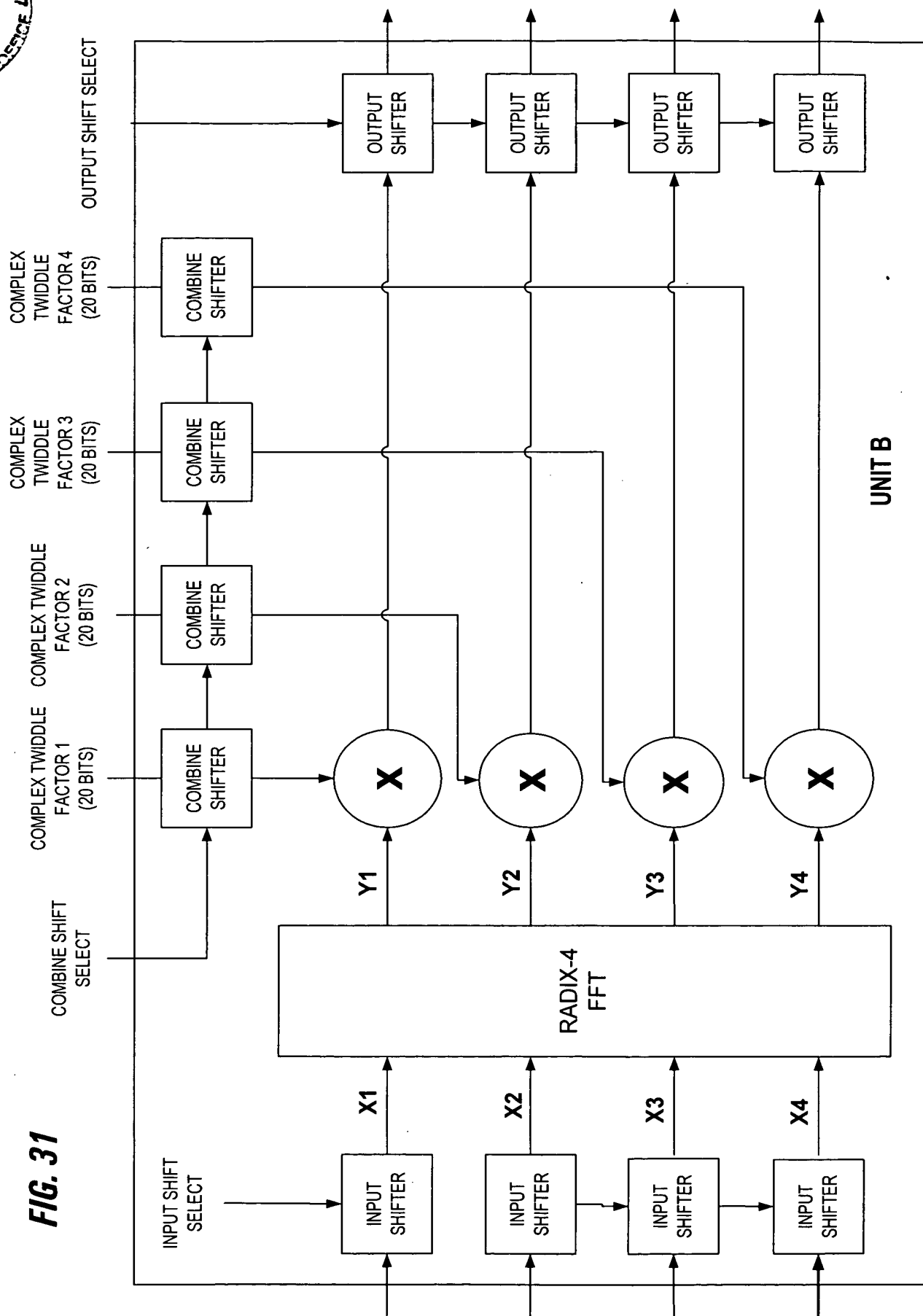


FIG. 30

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FIG. 31



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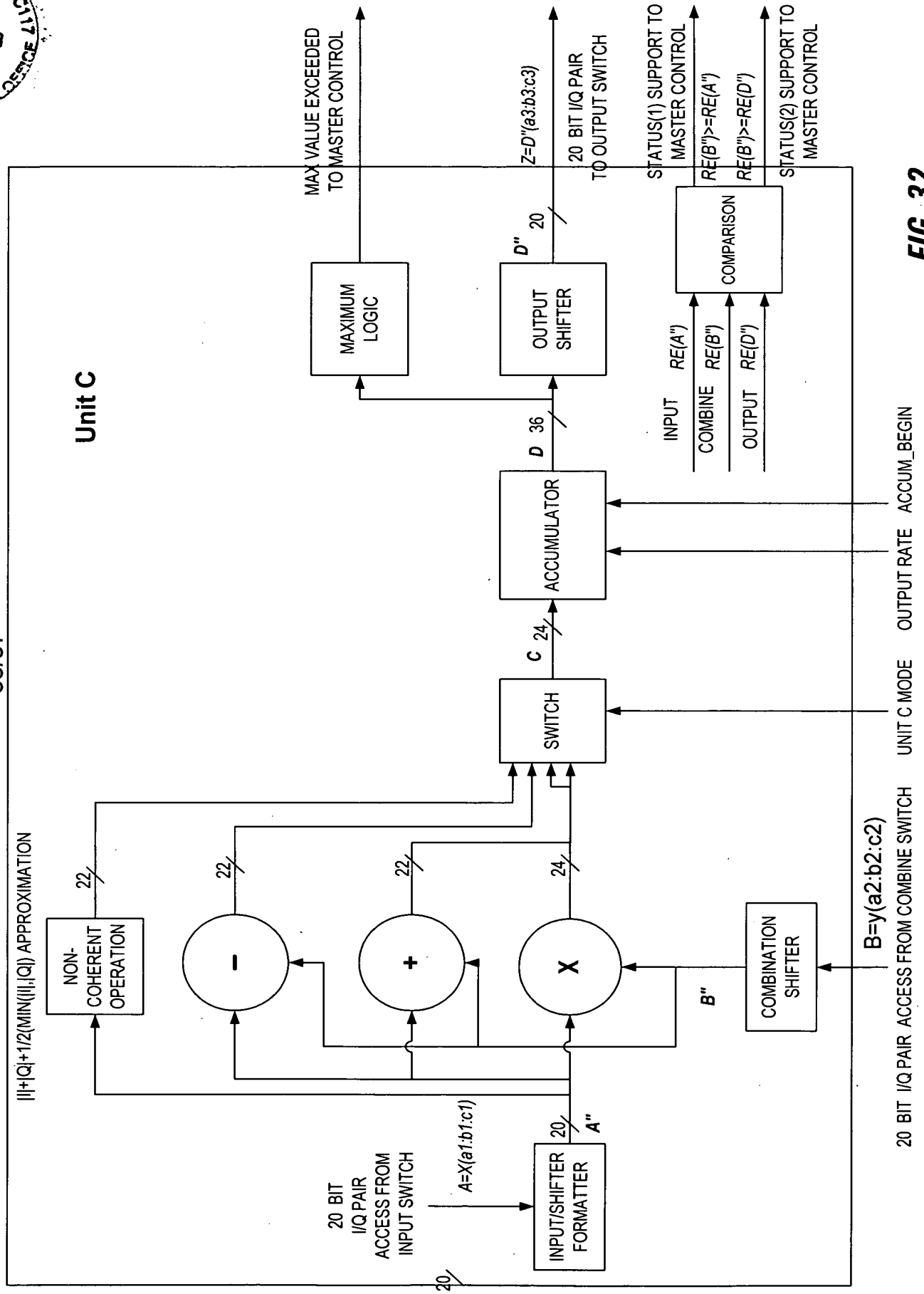


FIG. 32

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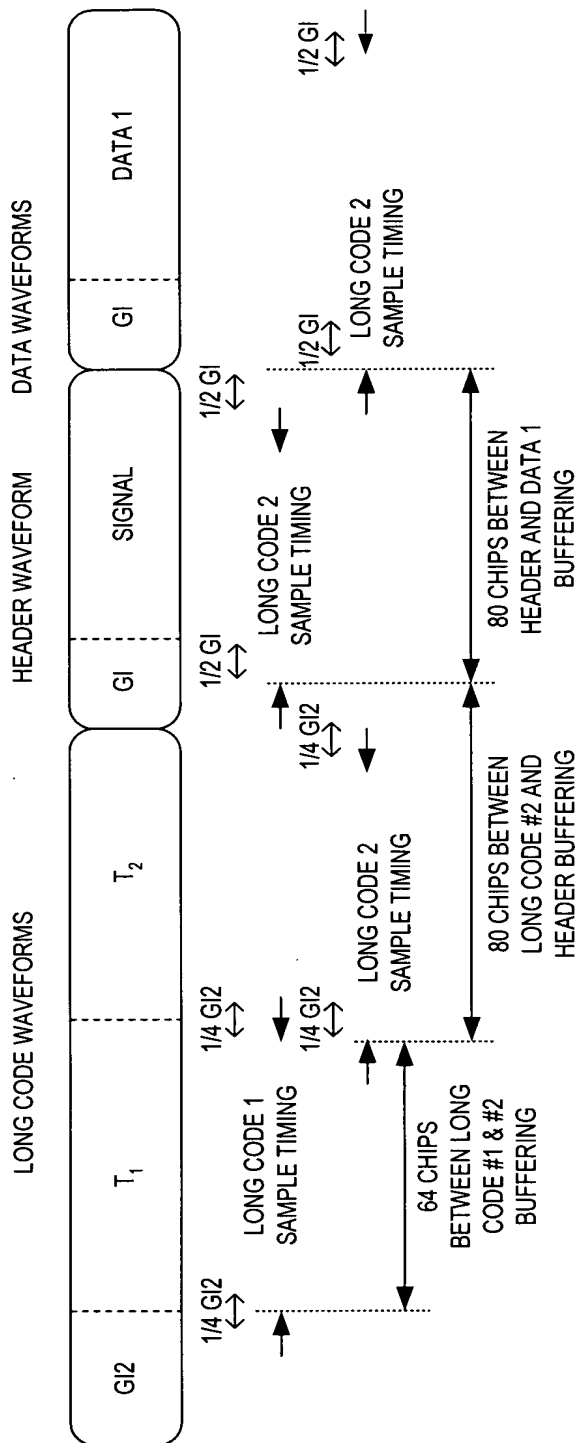


FIG. 33

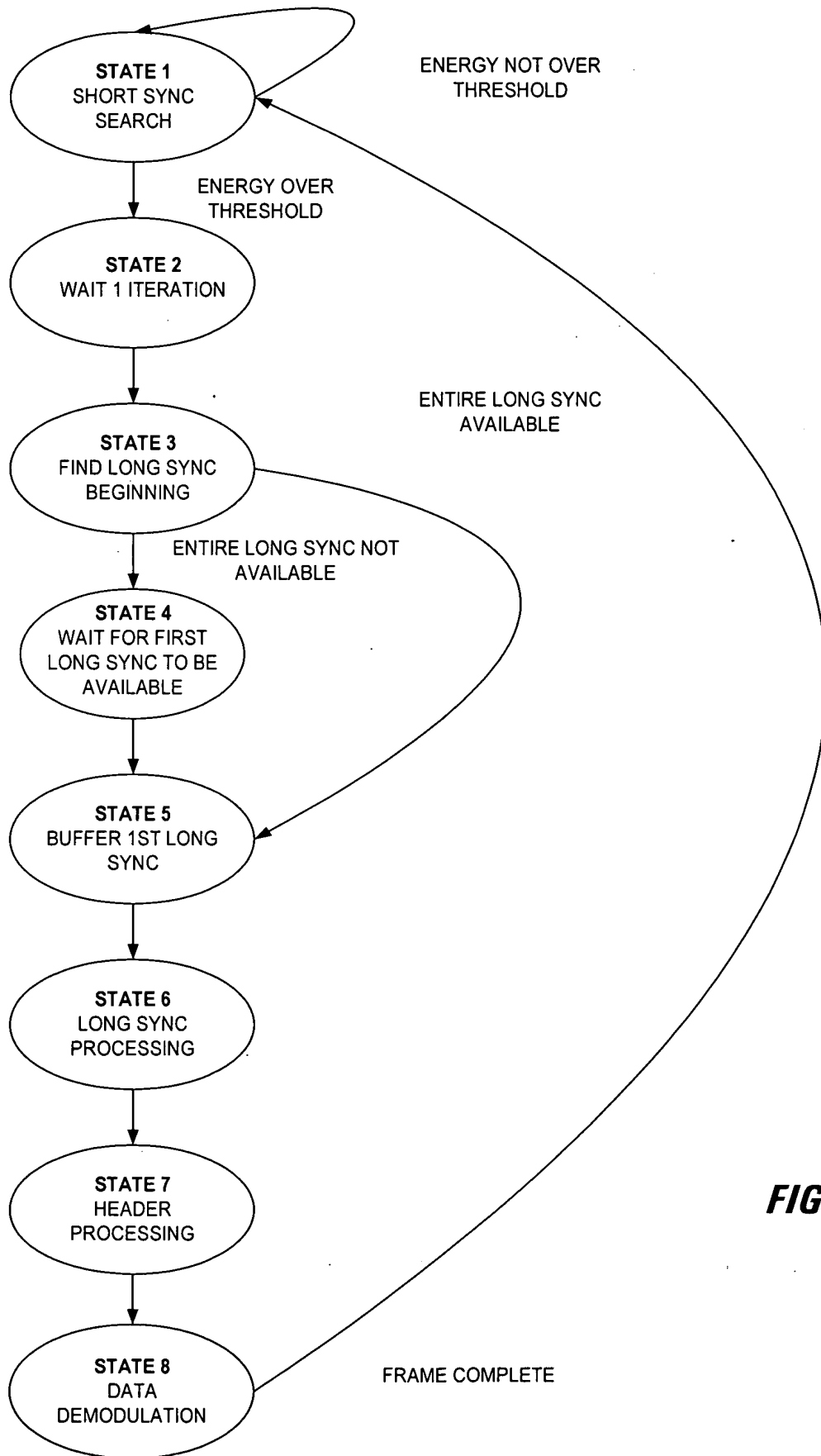


FIG. 34

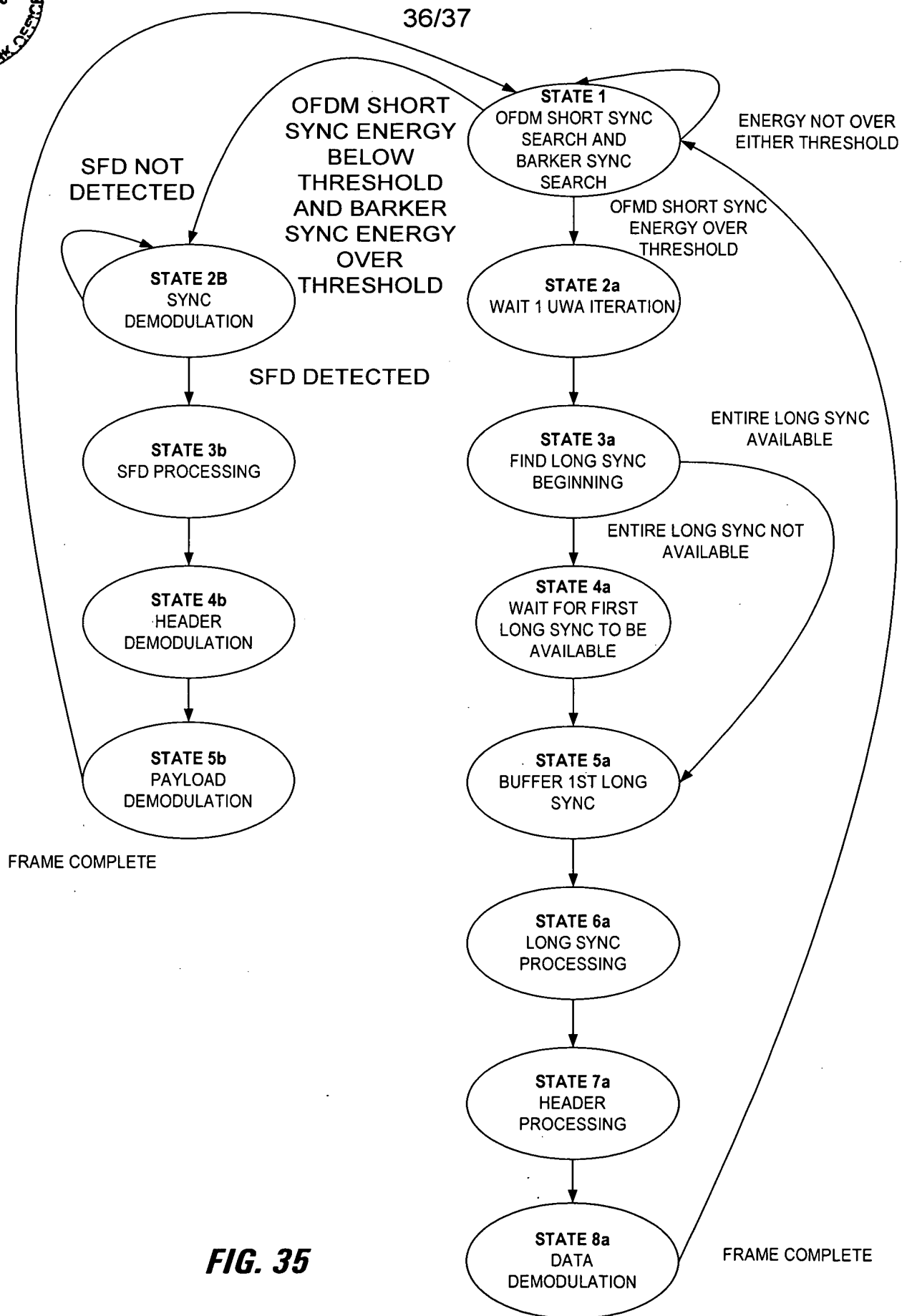


FIG. 35

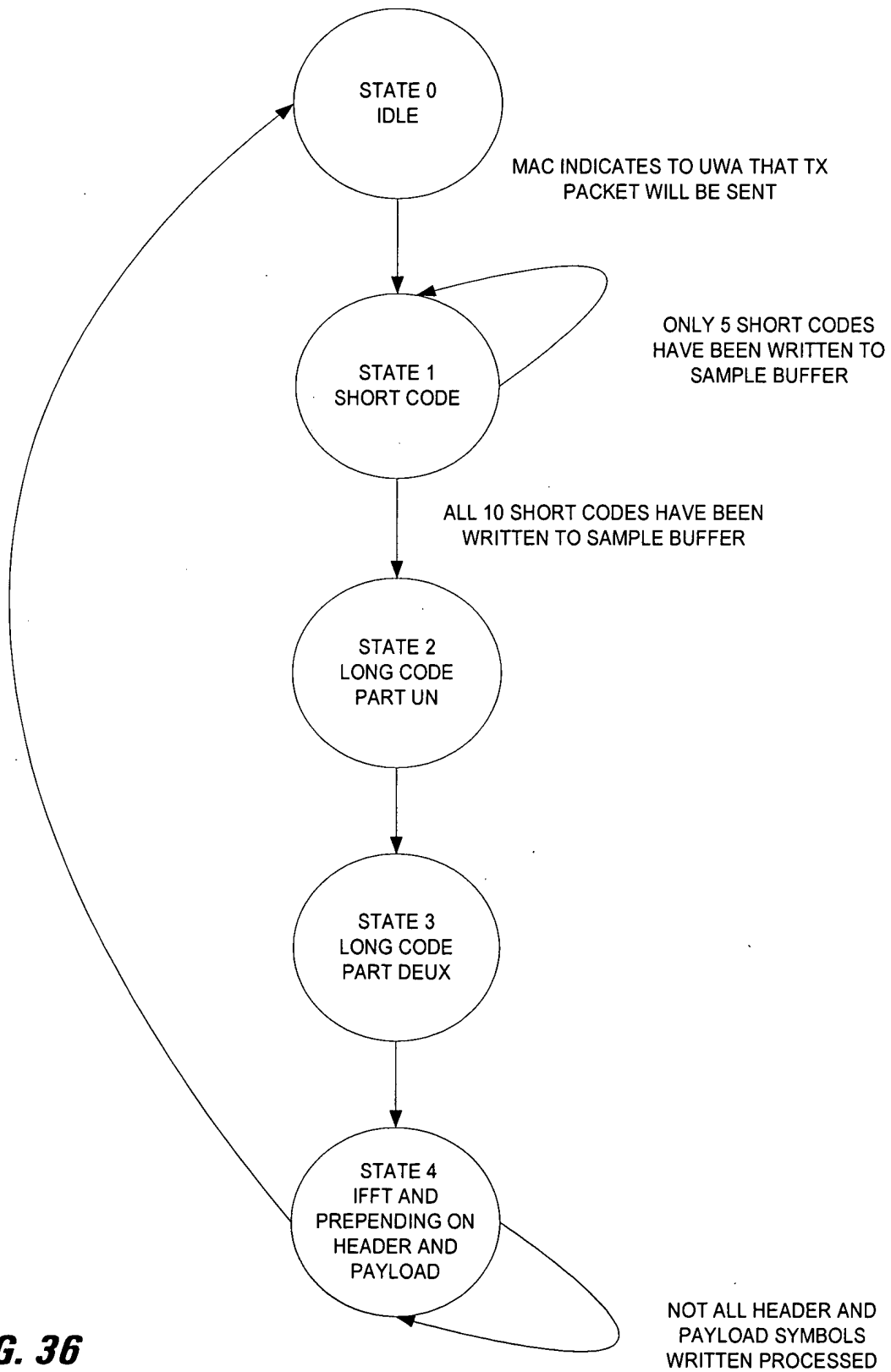


FIG. 36